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A new scheme for power factor correction and active filtering for six-pulse converters loads

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Abstract. This paper presents a novel harmonic-free power factor correction (PFC) topology based on T-type active power filter (APF), which is dedicated for power factor improvement and harmonic filtering for six-pulse converter loads. The cascaded controller structure is adopted for the proposed system, namely, the inner current loop and outer voltage loop. The current-loop control scheme is based on a decoupled state-space equations of the T-type APF using separate proportional-integral (PI) controllers in d-axis and q-axis of the synchronous rotating reference frame (SRRF) synchronized with grid voltages, respectively. The fundamental components of load-side currents are feed forwarded in the current-loop using two groups of synchronous frame adaptive linear neural networks (ADALINEs) to ensure estimation accuracy and a fast dynamic response. A separate proportional-integral (PI) controller is adopted in the outer voltage loop for balancing the active power flow of the voltage source inverter (VSI) dc-side capacitor. The experimental results confirm well with the theoretical analysis.

Key words: six-pulse converters, ADALINE, harmonic contamination, power factor correction, power quality.

1. Introduction

Power quality has become a research topic in power distribution systems due to a significant increase of harmonic pollution caused by proliferation of nonlinear loads, rectifiers, switching power supplies, and other grid connected power converters [1]. These nonlinear loads generate a large amount of characteristic harmonics and cause a low power factor, which deteriorate the electrical distribution systems. The proliferation of harmonics causes voltage distortion, additional losses and heating in the electrical equipments, perturbing torque, vibrations and noise in motors, malfunction and failures of sensitive equipments, resonances and electromagnetic interference (EMI) with electronic equipments. The simplest method to eliminate the characteristic harmonics and improve system power factor is to use passive filters tuned around the characteristic frequencies, such as 5^{th}, 7^{th}, 11^{th} or 13^{th} order harmonics. Whereas, passive filters are bulky, and they may detune with age, causes series or parallel resonance between line impedance and the passive components [2].

To overcome the drawbacks of passive filers, active power filers (APFs) are proposed in References [3–6] for harmonic and reactive power compensation. Normally, the shunt active power filters (SHAPFs) are used for current-source type nonlinear load, such as six-pulse rectifier with inductive load at dc-side. And series active power filters (SAPFs) are used for voltage-source type nonlinear load, such as six-pulse rectifier with capacitive load at dc-side. Unlike passive filters, active power filters have a tendency to destabilize at higher harmonic frequencies due to a broad bandwidth requirement of current control loop for shunt APF or voltage control loop for series APF, as discussed in Reference [5]. Moreover, it is shown in References [7, 8] that the shunt active filter is prone to instability when LC passive filters or power-factor correction (PFC) capacitor banks are connected on the load-side (downstream) from the point where the APF is connected. Similarly, dual stability characteristics also exist for series APF. Besides, shunt APF with capacitive rectifier load shows another type of trend which causes the instability of overall system. The mechanism is that the currents generated by APF flow into the diode/thyristor rectifier or load-side that presents low impedance, thus causing over-current of the load-side and increasing the harmonic current significantly. To reduce such sort of undesired interactions, a series inductor between shunt APF and the load is inevitable. Otherwise, total harmonic compensation is not theoretically achievable in presence of low leakage inductance of the main supply transformer [7].

This paper proposes a new power factor corrector (PFC) topology based on the T-type active power filter structure for harmonic and reactive compensation of six-pulse diode/thyristor converters, which exist in most of the front-end rectifier for ac-drive applications. By using the proposed topology, the stability problems of conventional shunt active power filter in case of compensating capacitive rectifier load can be eliminated. Different from the PFC topologies discussed in References [9–12], the proposed T-type active power filter is cascaded between the rectifier converter and the power distribution panel as the first power conversion stage. The tuned passive filter is shunt connected at the ac-side of the rectifier converter for the purpose of reducing the power rating of the voltage source inverter (VSI). This topology has the characteristic of decoupling the line impedance from the load impedance at higher frequencies, thus it has effective harmonic rejection capability at higher frequencies. The stability

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of the proposed system is ensured by reducing the controller bandwidth of the active T-type filter voltage source inverter (VSI). The presented topology has many advantages over the conventional shunt active power filters, such as, (a) total harmonic compensation can be implemented with simple control algorithm; (b) smaller bandwidth of sensors and controller; (c) it's immune to one cycle delay inherent in digital signal processor (DSP) or microcontroller implementation.

In the proposed harmonic-free PFC system, the compensating current of voltage source inverter (VSI) is minimized by properly designing of the passive filter parameters, such that the passive filter eliminates the majority of the dominant harmonics and compensates the fundamental reactive power required by the nonlinear load. The control objective of the proposed system is to achieve a nearly unity power factor (NUPF) and no harmonic current at source side. In the proposed control scheme, both source side and load side currents are sensed using current transducers (CTs). The inner current loop is responsible for fast current tracking, using proportional-integral controllers in d-axis and q-axis reference frame synchronized to the grid voltages by using a phase-locked-loop (PLL). The proportional-integral (PI) controllers are implemented in d-axis and q-axis based on the decoupled state-space equations of the T-type active power filter. The load side dynamics are incorporated in the feed-forward control loop by using two groups of synchronous frame adaptive linear neural networks (SADALINEs) [13–23] in d-axis and q-axis, respectively, for fast estimation of the fundamental components of nonlinear load currents. Besides, a separate proportional-integral (PI) controller is adopted in the outer voltage loop for balancing the active power flow of the voltage source inverter. On the basis of the proposed control scheme, the source side currents are controlled to track the reference currents instantaneously with a nearly unity power factor (NUPF) and no harmonics. The effectiveness of the proposed topology and its control schemes is validated by theoretical analysis and experimental results.

This remainder of this paper is outlined as follows. In Sec. 2, the power-stage circuit of the proposed topology and the original concept of harmonic compensation problem using the ADALINE-based control scheme are described. In Sec. 3, the stability characteristics of the proposed system in comparison with the conventional shunt active power filter (SHAPF) topologies are discussed. The mathematical model of the proposed system is given in Sec. 4. Then, the detailed control scheme based on the decoupled state-space equations of the T-type APF is presented in Sec. 5, where the adaptive linear neural networks (ADALINEs) are used to predict and minimized load-side disturbances. In Sec. 6, the experimental results under various load conditions are presented and compared with the EMI limits in the application. Finally, the main conclusions drawn in the paper are summarized in Sec. 7.

2. System description and problem statement

This Section first describes the circuit configuration of the proposed system. Then, the original concept of harmonic and reactive compensation problem using the ADALINE-based control scheme is introduced. As shown in Fig. 1, the proposed system is composed of three parts, conventional three-phase rectifier, a passive filter and a T-type active power filter. The passive filter is used for reducing the power rating of voltage source inverter (VSI) in T-type APF. It is tuned to eliminate the dominant harmonics by presenting a low-impedance path for the load current harmonics. The T-type APF is cascaded between rectifier load (rectifier load + shunt passive filter) and the distribution panel (marked as PCC in Fig. 1), acting as a narrow band-pass filter which exhibits high impedance path for the harmonic currents, thus the load and source impedances are decoupled at harmonic frequencies. The cascaded T-type APF is composed of a three-phase voltage source inverter (VSI) with dc-link capacitor, inductorsL_1 and L_2 at both sides of VSI.

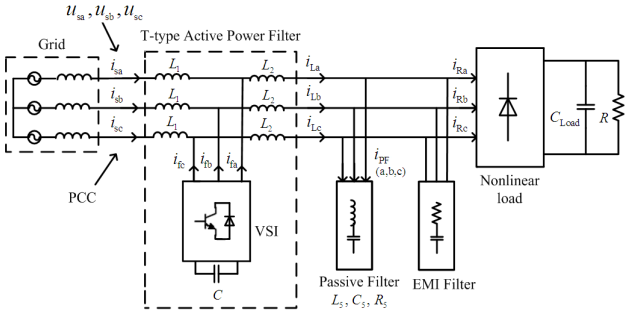

Fig. 1. Proposed harmonic-free power factor corrector topology based on T-type APF

Power factor correction (PFC) and harmonic compensation are realized simultaneously by programming the VSI output voltages of the T-type APF, such that the grid currents in the source-side arm of the T-type APF are controlled to follow a fundamental frequency sinusoidal wave shapes. The harmonic current entering the inductor L_2 bypasses to ground through the low impedance VSI. Furthermore, by designing a proper value of inductor L_2, the harmonic current sharing between the VSI and passive filter would be more effective for the proposed capacitive rectifier system. The poles resulted by shunt passive filter and L_2 interaction are placed at non-characteristic harmonic frequency to avoid undesired harmonic amplifications. Besides, the electromagnetic interference (EMI) filter composed of RC branch is shunt connected with the passive filter for switching ripples elimination generated by insulated gate bipolar transistors (IGBTs) of the voltage source inverter.

The problem formulation for the harmonic and reactive compensation of the proposed system using ADALINE-based approach is outlined as follows. In Fig. 1, the current at the load side of the T-type APF in phase 'a' can be expressed as

$$\begin{aligned} i_{\mathrm{La}} &= \sum_{n=1}^{\infty} I_{\mathrm{L,n}} \sin(n\omega_{\mathrm{s}} t + \varphi_{\mathrm{L,n}}) \\ &= I_{\mathrm{L,1}} \cos\varphi_{\mathrm{L,1}} \sin\omega_{\mathrm{s}} t + I_{\mathrm{L,1}} \sin\varphi_{\mathrm{L,1}} \cos\omega_{\mathrm{s}} t \\ &\quad + \sum_{n=2}^{\infty} I_{\mathrm{L,n}} \sin(n\omega_{\mathrm{s}} t + \varphi_{\mathrm{L,n}}) \\ &= i_{\mathrm{La,p}}(t) + i_{\mathrm{La,q}}(t) + i_{\mathrm{La,h}}(t), \end{aligned} \tag{1}$$

where ω_s is the angular frequency of the grid voltages, $\phi_{L,n}$ and $I_{L,n}$ are initial phase and amplitude of the n^{th} order harmonic component of the nonlinear load current, respectively. The currents $i_{La,p}(t)$, $i_{La,q}(t)$ and $i_{La,h}(t)$ are active, reactive and harmonic component of load side current, respectively. The same definition of source-side (grid) current in phase 'a' is expressed as

$$\begin{aligned} i_{sa} &= \sum_{n=1}^{\infty} I_{s,n} \sin(n\omega_s t + \varphi_{s,n}) \\ &= I_{s,1} \cos\varphi_{s,1} \sin\omega_s t + I_{s,1} \sin\varphi_{s,1} \cos\omega_s t \\ &\quad + \sum_{n=2}^{\infty} I_{s,n} \sin(n\omega_s t + \varphi_{s,n}) \\ &= i_{sa,p}(t) + i_{sa,q}(t) + i_{sa,h}(t), \end{aligned} \tag{2}$$

where $\phi_{s,n}$ and $I_{s,n}$ are initial phase and amplitude of the n^{th} order harmonic component of the source-side current, respectively. The currents $i_{sa,p}(t)$, $i_{sa,q}(t)$ and $i_{sa,h}(t)$ are active, reactive and harmonic component of the source side current, respectively.

The proposed harmonic-free power factor corrector can not only compensate harmonics generated by the rectifier converter, but also improve the power factor at source side. The source side power factor can be compensated to unity or nearly unity, depending on the philosophy of how to choose reference signal in current-loop controllers. For unity power factor (UPF) compensation strategy, the grid only supplies active fundamental current to the nonlinear rectifier load. The source-side current in phase 'a' can be expressed as

$$i^*_{sa}(t) = i_{La,p}(t) = I_{L,1} \cos\varphi_{L,1} \sin\omega_s t \tag{3}$$

Under this situation, the reactive and harmonic currents required by the load would be supplied by the T-type active power filter and the passive filter. As stated earlier, the passive filter is tuned to 5^{th} order harmonic frequency for attenuating the dominant 5^{th} order harmonic generated by the rectifier load, and also compensate a certain amount of reactive power, while the active filter compensate the rest of reactive and harmonic current. It should be noted that the passive filter can also be tuned to both 5^{th} and 7^{th} order harmonics, depending on the particular application. In this paper, only single tuned (ST) passive filter is considered for the sake of simplicity. The compensating current of the T-type APF can be expressed as

$$\begin{aligned} i_{fa}(t) &= i_{La,q}(t) + i_{La,h}(t) \\ &= I_{L,1} \sin\varphi_{L,1} \cos\omega_s t + \sum_{n=2}^{\infty} I_{L,n} \sin(n\omega_s t + \varphi_{L,n}). \end{aligned} \tag{4}$$

To achieve a nearly unity power factor (NUPF) at source-side is an alternative compensation objective. In order to reduce the power rating of the voltage source inverter, the target of achieving nearly unity power factor (NUPF) at source side is adopted in the following analysis and experimental setup. Under this assumption, the source side current can be expressed as

$$\begin{aligned} i^*_{sa}(t) &= i_{La,p}(t) + i_{La,q}(t) \\ &= I_{L,1} \cos\varphi_{L,1} \sin\omega_s t + I_{L,1} \sin\varphi_{L,1} \cos\omega_s t. \end{aligned} \tag{5}$$

Equation (5) shows that the source side supplies fundamental active and reactive current to the load. However, by optimizing the parameters of passive filter for full compensation of load-side fundamental reactive power, the reactive power absorbed from the grid can be very small, thus a nearly unity power factor (NUPF) at source side can be realized. Therefore, the compensating current of the T-type active filter can be expressed as

$$i_{fa}(t) = i_{La,h}(t) = \sum_{n=2}^{\infty} I_{L,n} \sin(n\omega_s t + \varphi_{L,n}). \tag{6}$$

As we know well, the scheme of reference signal generation (RSG) has a significant effect on the performance of active power filters (APFs) [3–8]. The inaccurate reference signal for the current control loop may result in poor compensation performance and further deteriorate the power quality at the distribution panel, which causes detrimental effects to the nearby customers connected at the point of common coupling (PCC). Besides, the time delay due to reference signal generation may cause instability of the active power filter under capacitive load [7]. Therefore, in order to accelerate the reference signal generation process and minimize the time delay due to mathematical manipulations, this paper aims to utilize the fast parallel processing capability of artificial neural networks (ANNs) to calculate the reference signals for the current loop controllers.

We shall first recall that the study of neural networks has received considerable attention in recent years, see, e.g. References [13–17], and references therein. Indeed, such networks are ideally suited for solving optimization problems. Many results on the existence and uniqueness of the equilibrium point, global asymptotic (exponential) stability have been established and applied to signal and image processing system, associate memories, pattern classification and so on. In Reference [13], cellular neural networks (CNNs) were used for tracking and obstacle avoidance in an autonomous robot. In References [14–15], the properties of global exponential convergence of discontinuous neural networks and delayed bidirectional associative memory neural networks (DBAMNN) were discussed. Then, in Reference [16], the convergence dynamics of general neural networks (GNNs) under almost periodic stimuli was investigated. In recent paper, single-layer perceptron (SLP) with an impulse activation function (IAF) and a dynamic neuron (DN) with a trapezoidal activation function (TAF) were used for linearly non-separable Boolean functions, which are a generalization of an SLP with hard limiter functions and CNN with a FAF [17]. The schemes presented in Reference [17] makes it possible to perform any real-world task described by a certain Boolean function via an SLP or a dynamic neuron. For a few years, ANN techniques have been widely explored for signal decomposition in electrical systems and are very promising in the field, as discussed in References [18–23]. Indeed, the learning capacities of the ANNs allow an online adaptation to every changing parameter of the electrical system, e.g., nonlinear and time-varying loads. The main motivation of this paper is to propose an adaptive linear neural network (ADALINE) approach for controlling the power elec-

tronic converters, which aims to facilitate reactive and harmonic compensation for nonlinear loads. This approach is motivated by a need of simplicity and flexibility in ANN-based control strategy used in electrical systems, but also to optimize the hardware resources required for the neural algorithmic implementation.

To achieve the target of pure sinusoidal wave shape in source current with a nearly unity power factor (NUPF), the distortion currents at the load-side are first identified by using adaptive linear neural networks (ADALINEs) to derive the reference signals for the source side currents. Considering the properties of three-phase systems, the three-phase quantities can be transformed into two-phase quantities in synchronous rotating reference frame (SRRF, or, $d-q$ reference frame) by applying Park's Transformations [24]. Hence two groups of ADALINEs are adopted in the d-axis and q-axis of the synchronous rotating frame to derive the *dc* components in $d-q$ reference frame, corresponding to the fundamental components of load currents in stationary phase $a-b-c$ frame. The drawbacks regarding to the sophisticated network structure and computational complexity in References [13–17] can be significantly simplified, which makes it possible to implement the algorithms in low cost digital signal processor (DSP) and facilitate the practical implementation of the proposed system.

In order to regulate the *dc*-link voltage of the voltages source inverter (VSI), the sensed *dc*-link voltage is subtracted by its reference value, and then the error signal is processed in the proportional-integral (PI) voltage controller (Fig. 5). The output of the *dc*-link voltage controller is used as the active current reference for the VSI. Consequently, the d-axis reference of the source side currents is obtained from summation of the output of voltage-loop controller and the *dc* component of the d-axis component of load-side currents. On the other hand, the q-axis reference of the source side currents is obtained from the *dc* component of the q-axis component of load side currents. In this way, the grid provides active power for the rectifier load and also a certain amount of active power to compensate the power loss of the VSI to sustain its *dc*-side voltage. The reactive power provided by the grid is very small for the rated load, and a nearly unity power factor (NUPF) can be achieved under a wide range of load variations. When the load is subject to disturbance, the real power between source side and load side is not sustained. The real power balance of the whole system is achieved by charging and discharging of *dc*-link capacitor of the voltage source inverter. The details regarding to the inner current-loop control and outer voltage-loop control are presented in Sec. 5.

3. Comparison of stability characteristics

This Section discusses the stability characteristics of the proposed system in comparison with the conventional shunt active power filter (SHAPF) topologies. Both theoretical analysis and quantization comparisons are presented for verification.

As stated earlier, the load and source interaction is a major cause of instability in series and shunt APF. To avoid this load and source interaction, a wide bandwidth current or voltage source inverter is required. Special control and pulse width modulation (PWM) techniques are usually suggested to achieve this target. For instance, in implementation of traditional shunt active power filter, the fast response of the current loop is utilized to inject the required compensating currents, whereas, as discussed in Reference [7], the inherent delay of the digital control system might result in poor stability margin at higher frequencies, especially in the application of thyristor or diode rectifier with capacitive load or a passive filter. In fact, when it is not possible to measure the purely distorting current I_d and the conventional compensation strategy, based on the total load current measurement, may imply the instability of the whole system if the load side includes a capacitive component [5, 7].

In contrast, the proposed harmonic-free PFC topology (Fig. 1) has the characteristic of decoupling the line impedance from the load impedance at higher frequencies, hence effectively resolving the issues of load sensitivity which are inherent in parallel and series APF. Since the voltages source inverter in Fig. 1 has low output impedance, the impedances of the load and the source do not interact with each other. Consequently, the resulting system is far less sensitive to load impedance. The remainder of this Section outlines the detailed comparison of stability characteristics between the conventional shunt APF topologies and the proposed harmonic-free PFC topology.

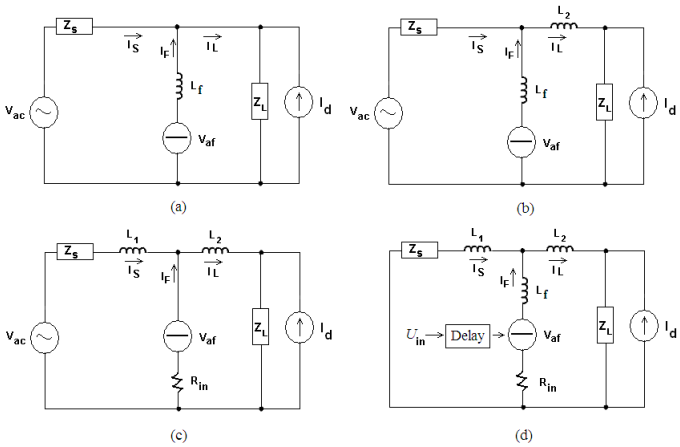

Fig. 2. Single phase representation of conventional shunt active power filters and the proposed PFC topology for stability analysis, a), b) conventional shunt active power filter topologies; c) proposed harmonic-free PFC topology; and d) the unified open-loop equivalent circuit of the conventional shunt active power filter topologies and the proposed topology

Figures 2a) and b) show the equivalent circuits of conventional shunt active power filter compensating a generic load. As discussed in earlier Sections, the topology in Fig. 2(a) has the poorest stability margin for capacitive load under control delay. To avoid undesired interaction between shunt APF and load impedance in case of compensating capacitive load, a series inductor L_2 can be inserted between shunt APF and the load, thus the topology in Fig. 2b) is derived [7]. In Fig. 2, the

power supply network is represented by an internal voltage $V_{\rm ac}$ with series impedance $Z_{\rm s}$ and the active filter is represented by a controller voltage source (CVS) $V_{\rm af}$ in series with an interfacing inductor $L_{\rm f}$. Hence the shunt active power filter works as controlled current source (CCS) which injects reactive and harmonic current to compensate the nonlinear load. A Norton equivalent circuit represents the nonlinear load, here the current generator $I_{\rm d}$ indicates the purely distorting load and the impedance $Z_{\rm L}$ represents passive components of the load, which may also include the possible capacitive load.

Once again, consider the system in Fig. 1. The impedance of the *dc*-link capacitor C (Fig. 1) can be considered quite small at harmonic frequencies, in comparison with load and line impedances. Hence its effect can be ignored. Under this assumption the VSI can be modeled as a controlled voltage source (CVS) with an effective power-stage impedance $R_{\rm in}$ of switches (conduction loss and switching losses). The resulting system with these assumptions is shown in Fig. 2c). Fig. 2d) shows the unified open-loop equivalent circuit of the conventional shunt active power filter topologies and the proposed PFC topology. The control input of VSI is represented by $U_{\rm in}$, with a delay due to digital sampling and PWM pattern calculations. Now we investigate the open-loop filtering properties of these topologies. Setting $V_{\rm af}$ equal to zero in Fig. 2d), the open-loop transfer function from the load disturbance to the source current is

$$G_1(s) = \frac{I_s\,(s)}{I_{\rm d}} = \frac{-Z_L(sL_{\rm f}+R_{\rm in})}{(sL_2+Z_{\rm L})\,(Z_1+sL_{\rm f}+R_{\rm in})+Z_1\,(sL_{\rm f}+R_{\rm in})}, \tag{7}$$

where, $Z_1 = sL_1 + Z_{\rm s}$. It should be noticed from Eq. (7) that the inductanceL_1 and L_2 equal to zero for the topology shown in Fig.2a), inductance L_1 equals to zero for the topology shown in Fig. 2b), and inductance $L_{\rm f}$ equals to zero for the topology shown in Fig. 2c).

By equating $L_{\rm f} = 0$, Eq. (7) can be expressed as

$$G_1(s) = \frac{I_{\rm s}\,(s)}{I_{\rm d}} = \frac{-Z_{\rm L}R_{\rm in}}{(sL_2+Z_{\rm L})\,(Z_1+R_{\rm in})+Z_1R_{\rm in}}, \tag{8}$$

which is the transfer function from the load disturbance to the source current for the proposed topology. For $R_{in} << 1$, it is easy to verify that the upper bound to Eq. (8) can be given by

$$I_{\rm s}\,(s) \approx \frac{-I_{\rm d}Z_{\rm L}R_{\rm in}}{(sL_2+Z_{\rm L})\,Z_1}. \tag{9}$$

From (9), it can be inferred, that the effect of any disturbance on the load side to source side current represents a low pass filter. Hence the effect of higher order harmonic disturbances will automatically attenuate to the source side thus the proposed topology is a natural filter to higher order harmonics. In practical inverters, the series resistance $R_{\rm in}$ of the inverter ranges in milliohms, thus by properly selection of L_1, the maximum value of $R_{\rm in}/L_1$ at harmonic frequencies can always be made much less than unity. Therefore, the effect of load-side disturbances can be minimized in the open-loop power stage design. This characteristic of the proposed topology plays an important role in achieving higher harmonic rejection at higher harmonic frequencies.

Figure 3 shows a comparison of frequency response from the load disturbance $I_{\rm d}$ to source side current $I_{\rm s}$ among the conventional SHAPF topologies (Fig. 2a) and b)) and the proposed PFC topology (Fig. 2c)). The system parameters under consideration are, $Z_{\rm s} = 0.02\ \Omega$, $L_1 = 500\ \mu$H, $L_2 = 1000\ \mu$H, $L_{\rm f} = 750\ \mu$H, internal resistance of VSI is assumed to be 0.1 Ω, switching frequency of IGBT is 10 kHz and the computation delay is 100 μs. It can be observed from Fig. 3 that the proposed topology has better attenuation at higher frequencies compared to the conventional SHAPF topologies. For instance, the magnitude-frequency plot of the conventional SHAPF topology shown in Fig. 2a) has an attenuation of 0.57 dB at 1.0 kHz and 0.22 dB at 2.0 kHz. Besides, the topology shown in Fig. 2b) has an attenuation of 6.9 dB at 1.0 kHz and 10.5 dB at 2.0 kHz. However, the proposed topology (Fig. 2c)) has an attenuation of 37.2 dB at 1.0 kHz and 47.7 dB at 2.0 kHz. Therefore, it is verified that the effect of higher order harmonic disturbances will be automatically attenuated to the source side. Hence the proposed topology is a natural filter to the higher order harmonics.

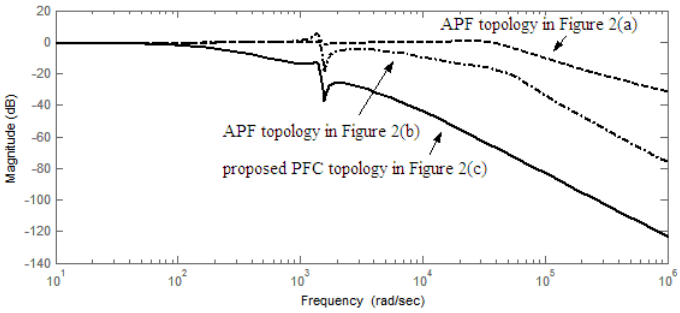

Fig. 3. Amplitude frequency response from load disturbance ($I_{\rm d}$) to source-side current ($I_{\rm s}$)

Next, we compare the system stability characteristics under control delay. Once again referring to Fig. 2d), the transfer function from the controlled voltage source (CVS) to the source current is given as

$$G_2(s) = \frac{I_{\rm s}\,(s)}{V_{\rm af}} = \frac{-(Z_{\rm L}+sL_2)}{Z_1\,(sL_2+Z_{\rm L})+(R_{\rm in}+sL_{\rm f})\,(Z_1+Z_{\rm L}+sL_2)}. \tag{10}$$

Considering $V_{\rm af} = -U_{\rm in}/(1+sT_{\rm d})$, where $U_{\rm in}$ is the input signal from the current controller and $T_{\rm d}$ is the delay in control loop. By equating $L_{\rm f} = 0$, the transfer function from the open-loop control to the output of the proposed system can be written as

$$G_3(s) = \frac{I_{\rm s}\,(s)}{U_{\rm in}} = \frac{(Z_{\rm L}+sL_2)}{\{Z_1\,(sL_2+Z_{\rm L})+R_{\rm in}\,(Z_1+Z_{\rm L}+sL_2)\}\,(1+sT_{\rm d})}. \tag{11}$$

From Eq. (11), it can be observed that this system can always be stabilized with a fixed controller for a broad range of linear load impedances if R_{in} is nearly equal to zero. However, if R_{in} is comparable with the load-side impedance, then the system may become unstable at higher frequencies for smaller values of capacitive load. Whereas, this situation does not arise in practical applications because the output of the APF is always filtered before being supplied to a load and this filtering requires a definite value of capacitor at the output. Hence the robustness and stability for a quite wide range of load can be achieved with a simple controller.

The open-loop bode diagram from the current controller input U_{in} to the source current I_{s} with control delay is shown in Fig. 4. It shows that the frequency-response of the conventional APF topology as indicated in Fig. 2a) has a gain margin of 52.9 dB and a phase margin of 95 degrees. And the frequency-response of the conventional APF topology as indicated in Fig. 2b) has a gain margin of 51.5 dB and phase margin of 93.9 degrees. In contrast, the frequency-response of the proposed topology has an infinite gain margin and a phase margin of 98 degrees. Therefore, it is confirmed that the proposed system has much higher stability margin at higher frequencies compared to the conventional SHAPF topologies. Besides, the infinite gain margin implies that the proposed system can be stabilized easily.

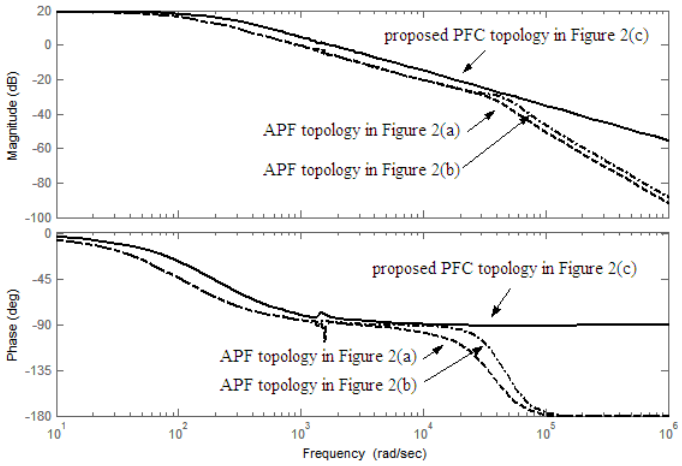

Fig. 4. Amplitude and phase frequency response from control input (U_{in}) to source-side current (I_{s})

4. System modeling

This Section formulates the mathematical model of the proposed T-type active power filter in order to derive the control law for the proposed system. Like any other dynamic system, the order of the proposed PFC system depends upon the number of the energy storage components which is definitely quite high. It has been shown in later part of this Section that the coupling among different branches of the T-type APF is not direct and is always made through the VSI *dc*-link. As the *dc*-link capacitor acts as a low-pass filter (LPF), its value is selected big enough in the design stage to minimize the interaction of the system and *dc*-link voltage regulation loop at higher frequencies. Consequently, the regulation of the voltage across this *dc*-link capacitor is made through a slow control loop at sub-harmonic level. Besides, the passive filter is selected in such a way that the poles and zeros of load side arm of the PFC lie quite above the fundamental frequency (about 5$^{\text{th}}$ order harmonic in the present design). Therefore, the load side (passive filter and the nonlinear load) has negligible effect on the dynamics of the line side inductors at higher frequencies and the dimension of the system model for control loop design can be reduced by modeling the source side arm of the T-type active power filter.

Once again referring to Fig. 1, the output phase-to-phase voltages of the VSI are defined as

$$u_{\text{iab}} = (f_1 - f_2)v_{\text{dc}}, \quad u_{\text{ibc}} = (f_2 - f_3)v_{\text{dc}}, \quad u_{\text{ica}} = (f_3 - f_1)v_{\text{dc}}, \tag{12}$$

where v_{dc} is *dc*-capacitor voltage of voltage source inverter, f_1, f_2 and f_3 are switching functions of each arm that the values are assumed to be zero or one according to the state of each converter arm, depending on the pulse patterns of the pulse width modulation (PWM) process. The phase voltages are derived as

$$u_{\text{ia}} = h_1 v_{\text{dc}}, \quad u_{\text{ib}} = h_2 v_{\text{dc}}, \quad u_{\text{ic}} = h_3 v_{\text{dc}}, \tag{13}$$

where the matrix of switching functions can be expressed as

$$H_{123} = \begin{bmatrix} h_1 \\ h_2 \\ h_3 \end{bmatrix} = \frac{1}{3}\begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix}\begin{bmatrix} f_1 \\ f_2 \\ f_3 \end{bmatrix}, \tag{14}$$

assuming the switching function h_1, h_2 and h_3 are 0, $\pm$1/3 and $\pm$2/3. To attain total harmonic compensation, the voltage across inductor L_1 should not have any harmonic component. Consequently, the output voltages of VSI are always sinusoids of fundamental components. Under this assumption, the state-space equations for the source-side currents are

$$\begin{bmatrix} \frac{di_{\text{sa}}}{dt} \\ \frac{di_{\text{sb}}}{dt} \\ \frac{di_{\text{sc}}}{dt} \end{bmatrix} = \begin{bmatrix} -\frac{R_{\text{a}}}{L_1} & 0 & 0 & -\frac{h_1}{L_1} \\ 0 & -\frac{R_{\text{a}}}{L_1} & 0 & -\frac{h_2}{L_1} \\ 0 & 0 & -\frac{R_{\text{a}}}{L_1} & -\frac{h_3}{L_1} \end{bmatrix}\begin{bmatrix} i_{\text{sa}} \\ i_{\text{sb}} \\ i_{\text{sc}} \\ v_{\text{dc}} \end{bmatrix} + \begin{bmatrix} \frac{u_{\text{sa}}}{L_1} \\ \frac{u_{\text{sb}}}{L_1} \\ \frac{u_{\text{sc}}}{L_1} \end{bmatrix}, \tag{15}$$

where R_{a} is equivalent parasitic resistance of inductance L_1, and u_{sa}, u_{sb} and u_{sc} are source side voltages sensed using potential transducers (PTs). Applying Park's Transformation (16) to Eq. (15), the state-space equations in synchronous rotating reference frame (SRRF) can be expressed as Eq. (17)

$$C_{\text{dq0}}^{\text{abc}} = \sqrt{\frac{2}{3}}\begin{bmatrix} \cos\omega_{\text{s}}t & \cos\left(\omega_{\text{s}}t - \frac{2\pi}{3}\right) & \cos\left(\omega_{\text{s}}t + \frac{2\pi}{3}\right) \\ -\sin\omega_{\text{s}}t & -\sin\left(\omega_{\text{s}}t - \frac{2\pi}{3}\right) & -\sin\left(\omega_{\text{s}}t + \frac{2\pi}{3}\right) \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix}, \tag{16}$$

$$\begin{bmatrix} \frac{di_{\rm sd}}{dt} \\ \frac{di_{\rm sq}}{dt} \end{bmatrix} = \begin{bmatrix} -\frac{R_{\rm a}}{L_1} & \omega & -\frac{h_1}{L_1} \\ -\omega & -\frac{R_{\rm a}}{L_1} & -\frac{h_2}{L_1} \end{bmatrix} \begin{bmatrix} i_{\rm sd} \\ i_{\rm sq} \\ v_{\rm dc} \end{bmatrix} + \begin{bmatrix} \frac{u_{\rm d}}{L_1} \\ \frac{u_{\rm q}}{L_1} \end{bmatrix}, \tag{17}$$

where $u_{\rm d}$, $u_{\rm q}$ are source-side voltages and $i_{\rm sd}$, $i_{\rm sq}$ are source-side currents in synchronous rotating reference frame. And $\omega_{\rm s}$ is the angular frequency of grid voltages. According to Kirchoff's law, the current of the VSI *dc*-side capacitor satisfies Eq. (18)

$$C\frac{dv_{\rm dc}}{dt} = i_{\rm dc} = h_1 i_{\rm fa} + h_2 i_{\rm fb} + h_3 i_{\rm fc}, \tag{18}$$

where $i_{\rm fa}$, $i_{\rm fb}$ and $i_{\rm fc}$ are VSI currents, and C is the capacitance of VSI *dc*-side capacitor. Applying coordinate transformation (16) to Eq. (17), the following equation is obtained

$$\begin{aligned} \frac{dv_{\rm dc}}{dt} &= \frac{1}{C}\begin{bmatrix} h_1 & h_2 & h_3 \end{bmatrix} \begin{bmatrix} i_{\rm La} - i_{\rm sa} \\ i_{\rm Lb} - i_{\rm sb} \\ i_{\rm Lc} - i_{\rm sc} \end{bmatrix} \\ &= \frac{1}{C}[C_{\rm abc}^{\rm dq0} H_{\rm dq0}]^{\rm T} \cdot C_{\rm abc}^{\rm dq0}[i_{\rm Ldq0} - i_{\rm sdq0}] \\ &= \frac{1}{C} H_{\rm dq0}^{\rm T} \cdot [i_{\rm Ldq0} - i_{\rm sdq0}] \\ &= -\frac{h_{\rm d}}{C} i_{\rm sd} - \frac{h_{\rm q}}{C} i_{\rm sq} + \frac{h_{\rm d} i_{\rm Ld} + h_{\rm q} i_{\rm Lq}}{C}, \end{aligned} \tag{19}$$

where $i_{\rm Ld}$ and $i_{\rm Lq}$ are load side currents in synchronous rotating frame, $C_{\rm abc}^{\rm dq0}$ represents inverse Park's transformation. The variables $h_{\rm d}$ and $h_{\rm q}$ are computed from h_1, h_2 and h_3 the same way as $i_{\rm sd}$ and $i_{\rm sq}$ are computed from $i_{\rm sa}$, $i_{\rm sb}$ and $i_{\rm sc}$. Eq. (19) shows that the load side currents affect the system state-space equations through the *dc*-link capacitor and there is no direct coupling between the load side and source side currents. The main objective of the proposed system is to control the VSI output voltages such that the currents in L_1 are equal to the fundamental components in the load side arm. Under this assumption, the theoretical power exchange at harmonic frequency will be zero, hence it will not affect the *dc*-link voltage. Consequently, the high frequency dynamics of the load arm have negligible effect on the source side arm dynamics. Therefore, by combining Eqs. (17) and (19), the complete state-space equation of the system is derived as

$$\begin{bmatrix} \frac{di_{\rm sd}}{dt} \\ \frac{di_{\rm sq}}{dt} \\ \frac{dv_{\rm dc}}{dt} \end{bmatrix} = \begin{bmatrix} -\frac{R_{\rm a}}{L_1} & \omega & -\frac{h_{\rm d}}{L_1} \\ -\omega & -\frac{R_{\rm a}}{L_1} & -\frac{h_{\rm q}}{L_1} \\ -\frac{h_{\rm d}}{C} & -\frac{h_{\rm q}}{C} & 0 \end{bmatrix} \begin{bmatrix} i_{\rm sd} \\ i_{\rm sq} \\ v_{\rm dc} \end{bmatrix} + \begin{bmatrix} \frac{u_{\rm d}}{L_1} \\ \frac{u_{\rm q}}{L_1} \\ \frac{i_{\rm dis}}{C} \end{bmatrix}. \tag{20}$$

Here $i_{\rm dis}$ represents the term $h_{\rm d} i_{\rm Ld} + h_{\rm q} i_{\rm Lq}$ in Eq. (19), which is an approximation of load side dynamics, considering *dc*-link capacitor of VSI big enough. A better system model can be obtained by writing the state-space equations considering the load side arm, but no such effort will be made over here. Instead, a feed-forward loop based on synchronous frame adaptive linear neural network (SADALINE) is adopted to predict and minimize the effect of load side disturbances. Using the controller presented by Eq. (21), decoupling between d-axis and q-axis is achieved by using the new inputs $U_{\rm d}$ and $U_{\rm q}$.

$$\left.\begin{aligned} U_{\rm d} &= u_d - h_{\rm d} v_{\rm dc} + \omega L_1 i_{\rm sq} \\ U_{\rm q} &= u_{\rm q} - h_{\rm q} v_{\rm dc} - \omega L_1 i_{\rm sd} \end{aligned}\right\}. \tag{21}$$

Substituting Eq. (21) back to Eq. (20), the decoupled system model is obtained as

$$\begin{bmatrix} \frac{di_{\rm sd}}{dt} \\ \frac{di_{\rm sq}}{dt} \end{bmatrix} = \begin{bmatrix} -\frac{R_{\rm a}}{L_1} & 0 \\ 0 & -\frac{R_{\rm a}}{L_1} \end{bmatrix} \begin{bmatrix} i_{\rm sd} \\ i_{\rm sq} \end{bmatrix} + \begin{bmatrix} \frac{1}{L_1} & 0 \\ 0 & \frac{1}{L_1} \end{bmatrix} \begin{bmatrix} U_{\rm d} \\ U_{\rm q} \end{bmatrix}, \tag{22}$$

$$\frac{dv_{\rm dc}}{dt} = \frac{U_{\rm d} - u_{\rm d}}{C v_{\rm dc}} i_{\rm sd} + \frac{U_{\rm q} - u_{\rm q}}{C v_{\rm dc}} i_{\rm sq} + \frac{i_{\rm dis}}{C}. \tag{23}$$

5. Control schemes

As stated earlier in Sec. 2, the control objective of the proposed harmonic free power factor corrector is to eliminate harmonics, achieve nearly unity power factor (NUPF) at the source side and regulate *dc*-side voltage of the voltage source inverter. The hierarchical controller structure is adopted in this paper, namely, the output of outer voltage loop is used as reference signal in the inner current loop. The current loop controller is based on the source-side state-space equations and load current feed forward using two groups of synchronous frame adaptive linear neural networks (SADALINEs). The proportional-integral controller is employed in the outer voltage loop for balancing active power flow of the voltage source inverter. The following Subsections outline the detailed control schemes of the proposed system. We first introduce the current loop control in Subsec. 5.1. Then, a detailed mathematical formulation of adaptive linear neural network (ADALINE) is presented in Subsec. 5.2. And the outer voltage loop control is discussed in Subsec. 5.3.

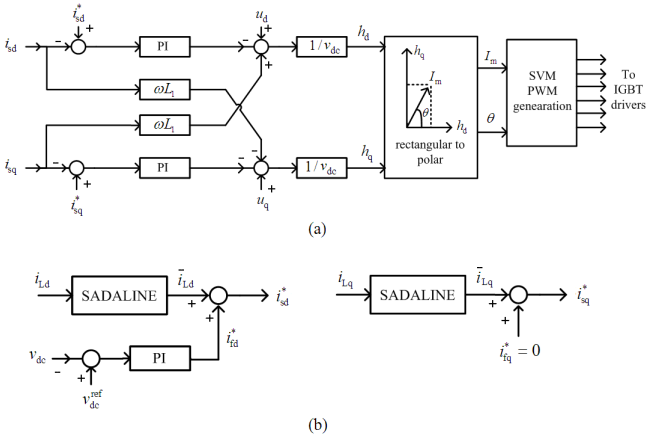

Fig. 5. Block diagram of control scheme for the proposed PFC system, a) decoupled current loop controller in d-axis and q-axis and b) reference signal generation method in d-axis and q-axis

5.1. Current loop control. Figure 5a) shows the diagram of control scheme derived from the Eqs. (20)–(23). The decoupling between d-axis and q-axis can be achieved by controlling the new input U_d and U_q. Since decoupling is achieved, proportional-integral controllers can be applied to regulate the real and reactive power in d-axis and q-axis respectively, which can be expressed as

$$\left.\begin{aligned} U_\mathrm{d} &= \left(k_\mathrm{pcc} + k_\mathrm{icc}\frac{1}{s}\right)(i^*_\mathrm{sd} - i_\mathrm{sd}) \\ U_\mathrm{q} &= \left(k_\mathrm{pcc} + k_\mathrm{icc}\frac{1}{s}\right)(i^*_\mathrm{sq} - i_\mathrm{sq}) \end{aligned}\right\}, \tag{24}$$

where k_pcc and k_icc are proportional and integral gains of current loop controller, respectively. Equation (21) shows that the switching function in d-axis and q-axis can be expressed as

$$\left.\begin{aligned} h_\mathrm{d} &= \frac{1}{v_{textrmdc}}(u_\mathrm{d} - U_\mathrm{d} + \omega L_1 i_\mathrm{sq}) \\ h_\mathrm{q} &= \frac{1}{v_\mathrm{dc}}(u_\mathrm{q} - U_\mathrm{q} - \omega L_1 i_\mathrm{sd}) \end{aligned}\right\}. \tag{25}$$

The obtained switching functions h_d and h_q are transformed into polar coordinates to get the PWM modulation index I_m and power angle θ for generation of PWM signals to drive the power semiconductors (IGBTs) of the voltage source inverter. Fig. 5b) shows that the reference signal in d-axis and q-axis current loop controller can be expressed as

$$\left.\begin{aligned} i^*_\mathrm{sd} &= \overline{i}_\mathrm{Ld} + i^*_\mathrm{fd} \\ i^*_\mathrm{sq} &= \overline{i}_\mathrm{Lq} \end{aligned}\right\}, \tag{26}$$

where $\overline{i}_\mathrm{Ld}$ and $\overline{i}_\mathrm{Lq}$ are dc components of load side currents in $d-q$frame synchronized with the grid voltages, corresponding to the fundamental components of load side currents. The load side fundamental components $\overline{i}_\mathrm{Ld}$ and $\overline{i}_\mathrm{Lq}$ are obtained by using adaptive linear neural network for fast tracking of load side dynamics, which would be discussed in detail in the following Subsection. And i^*_fd is the output of dc-voltage loop controller, corresponding to active power loss of the voltage source inverter.

5.2. Load currents feed-forward using neural networks. In this Subsection, the mathematical formulation of adaptive linear neural network (ADALINE) [18–23] is outlined as follows. Consider an arbitrary signal$Y(t)$ with Fourier series expansion as

$$\begin{aligned} Y(t) &= \sum_{n=0,1,2,3,\cdots}^{N} A_\mathrm{n}\sin(n\omega t + \phi_\mathrm{n}) + \varepsilon(t) \\ &= \sum_{n=0,1,2,3,\cdots}^{N} (a_\mathrm{n}\sin 2\pi nft + b_\mathrm{n}\cos 2\pi nft) + \varepsilon(t), \end{aligned} \tag{27}$$

where A_n and φ_n are correspondingly the amplitude and phase angle of the n^th order harmonic component, and $\varepsilon(t)$ represents higher order components and random noise. In order to formulate the harmonic estimation problem by using ADALINE, we firstly define the pattern vector X_k and weight vector W_k as

$$X_\mathrm{k} = [1, \sin\omega t_\mathrm{k}, \cos\omega t_\mathrm{k}, \cdots, \sin N\omega t_\mathrm{k}, \cos N\omega t_\mathrm{k}\ ]^\mathrm{T}, \tag{28}$$

$$W_\mathrm{k} = [b^\mathrm{k}_0,\, a^\mathrm{k}_1,\, b^\mathrm{k}_1,\, a^\mathrm{k}_2,\, b^\mathrm{k}_2, ..., a^\mathrm{k}_\mathrm{N}, b^\mathrm{k}_\mathrm{N}]^\mathrm{T} \tag{29}$$

The square error on the pattern X_k is expressed as

$$\begin{aligned} \varepsilon_\mathrm{k} &= \frac{1}{2}(d_\mathrm{k} - X^\mathrm{T}_\mathrm{k}W_\mathrm{k})^2 = \frac{1}{2}e^2_\mathrm{k} \\ &= \frac{1}{2}(d^2_\mathrm{k} - 2d_\mathrm{k}X^T_\mathrm{k}W_\mathrm{k} + W^\mathrm{T}_\mathrm{k}X_\mathrm{k}X^\mathrm{T}_\mathrm{k}W_\mathrm{k}), \end{aligned} \tag{30}$$

where d_k is the desired scalar output. The mean-square error (MSE) ε can be obtained by calculating the expectation of both sides of Eq. (30), as

$$\varepsilon = E[\varepsilon_\mathrm{k}] = \frac{1}{2}E[d^2_\mathrm{k}] - E[d_\mathrm{k}X^\mathrm{T}_\mathrm{k}]W_\mathrm{k} + \frac{1}{2}W^\mathrm{T}_\mathrm{k}E[X_\mathrm{k}X^\mathrm{T}_\mathrm{k}]W_\mathrm{k}, \tag{31}$$

where the weights are assumed to be fixed at W_k while computing the expectation. The objective of the adaptive linear neural network (ADALINE) is to find the optimal weight vector $\hat{W}_\mathrm{k}$ that minimizes the MSE of Eq. (31). For convenience of expression, Eq. (31) is rewritten as [18]

$$\varepsilon = E[\varepsilon_\mathrm{k}] = \frac{1}{2}E[d^2_\mathrm{k}] - P^TW_\mathrm{k} + \frac{1}{2}W^\mathrm{T}_\mathrm{k}\mathbf{R}W_\mathrm{k}, \tag{32}$$

where P^T and $\mathbf{R}$ are defined as

$$\begin{aligned} P^\mathrm{T} &= E[d_\mathrm{k}X^\mathrm{T}_\mathrm{k}] \\ &= E[(d_\mathrm{k}, d_\mathrm{k}\sin\omega t_\mathrm{k}, d_\mathrm{k}\cos\omega t_\mathrm{k}, ..., d_\mathrm{k}\sin N\omega t_\mathrm{k}, d_\mathrm{k}\cos N\omega t_\mathrm{k})], \end{aligned} \tag{33}$$

$$\begin{aligned} \mathbf{R} &= E[X_\mathrm{k}X^\mathrm{T}_\mathrm{k}] \\ &= E\begin{bmatrix} 1 & \sin\omega t_\mathrm{k} & \dots & \cos N\omega t_\mathrm{k} \\ \sin\omega t_\mathrm{k} & \sin\omega t_\mathrm{k}\sin\omega t_\mathrm{k} & \dots & \sin\omega t_\mathrm{k}\cos N\omega t_\mathrm{k} \\ \dots & \dots & \dots & \dots \\ \cos N\omega t_\mathrm{k} & \cos N\omega t_\mathrm{k}\sin\omega t_\mathrm{k} & \dots & \cos N\omega t_\mathrm{k}\cos N\omega t_\mathrm{k} \end{bmatrix}. \end{aligned} \tag{34}$$

Notably, matrix $\mathbf{R}$ is real and symmetric, and ε is a quadratic function of weights. The gradient function $\nabla\varepsilon$ corresponding to the MSE function of Eq. (32) is obtained by straightforward differentiation

$$\nabla\varepsilon = \left(\frac{\partial\varepsilon}{\partial b^\mathrm{k}_0}, \frac{\partial\varepsilon}{\partial a^\mathrm{k}_1}, \frac{\partial\varepsilon}{\partial b^\mathrm{k}_1}, ..., \frac{\partial\varepsilon}{\partial a^\mathrm{k}_N}, \frac{\partial\varepsilon}{\partial b^\mathrm{k}_N}\right)^\mathrm{T} = -P + \mathbf{R}W_\mathrm{k}, \tag{35}$$

which is a linear function of weights. The optimal set of weights, $\hat{W}_\mathrm{k}$, can be obtained by setting $\nabla\varepsilon = 0$, which yields

$$-P + \mathbf{R}\hat{W}_\mathrm{k} = 0. \tag{36}$$

The solution of the Eq. (36) is called Weiner solution or the Weiner filter

$$\hat{W}_\mathrm{k} = \mathbf{R}^{-1}P. \tag{37}$$

The Weiner solution corresponds to the point in weight space that represents the minimum mean-square error ε_min.

To compute the optimal filter one must first compute $\mathbf{R}^{-1}$ and P. However, it would be difficult to compute $\mathbf{R}^{-1}$ and P accurately when the input data comprises a random stream of patterns (drawn from a stationary distribution). Thus, by direct calculating gradients of the square error (Eq. (30)) at the k^{th} iteration

$$\begin{aligned}\tilde{\nabla}\varepsilon_{\mathrm{k}} &= \left(\frac{\partial\varepsilon_{\mathrm{k}}}{\partial b_0^{\mathrm{k}}},\ \frac{\partial\varepsilon_{\mathrm{k}}}{\partial a_1^{\mathrm{k}}},\ \frac{\partial\varepsilon_{\mathrm{k}}}{\partial b_1^{\mathrm{k}}},\ ...,\ \frac{\partial\varepsilon_{\mathrm{k}}}{\partial a_{\mathrm{N}}^{\mathrm{k}}},\ \frac{\partial\varepsilon_{\mathrm{k}}}{\partial b_{\mathrm{N}}^{\mathrm{k}}}\right)^{\mathrm{T}} \\ &= e_{\mathrm{k}}\left(\frac{\partial e_{\mathrm{k}}}{\partial b_0^{\mathrm{k}}},\ \frac{\partial e_{\mathrm{k}}}{\partial a_1^{\mathrm{k}}},\ \frac{\partial e_{\mathrm{k}}}{\partial b_1^{\mathrm{k}}},\ ...,\ \frac{\partial e_{\mathrm{k}}}{\partial a_{\mathrm{N}}^{\mathrm{k}}},\ \frac{\partial e_{\mathrm{k}}}{\partial b_{\mathrm{N}}^{\mathrm{k}}}\right) = -e_{\mathrm{k}}X_{\mathrm{k}},\end{aligned} \tag{38}$$

where $e_{\mathrm{k}} = (d_{\mathrm{k}} - s_{\mathrm{k}})$, and $s_{\mathrm{k}} = X_{\mathrm{k}}^{\mathrm{T}}W_{\mathrm{k}}$ since we are dealing with linear neurons.

Therefore, the recursive weights updating equation can be expressed as

$$W_{\mathrm{k}+1} = W_{\mathrm{k}} + \mu(-\tilde{\nabla}\varepsilon_{\mathrm{k}}) = W_{\mathrm{k}} + \mu e_{\mathrm{k}}X_{\mathrm{k}} = W_{\mathrm{k}} + \mu(d_{\mathrm{k}} - s_{\mathrm{k}})X_{\mathrm{k}}, \tag{39}$$

where the learning rate μ is used to adjust the convergence speed and the stability of weights updating process. Taking the expectation of Eq. (38), the following equation is derived

$$\begin{aligned}E[\tilde{\nabla}\varepsilon_{\mathrm{k}}] &= -E[e_{\mathrm{k}}X_k] = -E[d_{\mathrm{k}}X_{\mathrm{k}} - X_{\mathrm{k}}X_{\mathrm{k}}^{\mathrm{T}}W_{\mathrm{k}}] \\ &= \mathbf{R}W_{\mathrm{k}} - P = \nabla\varepsilon.\end{aligned} \tag{40}$$

From Eq. (40), it can be found that the long-term average of $\tilde{\nabla}\varepsilon_{\mathrm{k}}$ approaches $\nabla\varepsilon$ hence $\tilde{\nabla}\varepsilon_{\mathrm{k}}$ can be used as unbiased estimate of $\nabla\varepsilon$. If the input data set is finite (deterministic), then the gradient $\nabla\varepsilon$ can be computed accurately by collecting the different $\tilde{\nabla}\varepsilon_{\mathrm{k}}$ gradients over all training patterns X_{k} for the same set of weights. The steepest descent search is guaranteed to search the Weiner solution provided the learning rate condition Eq. (41) is satisfied [18]

$$0 < \mu < \frac{2}{\lambda_{\max}}, \tag{41}$$

where $\lambda_{\max}$ represents the largest eigenvalue of $\mathbf{R}$. As for learning rate μ, increasing it results in a faster convergence at the trade-off of losing accuracy and increasing overshoots in transient response. Theoretically, a dynamical learning rate has better convergence, however, the implementation will be more demanding and requires more expensive hardware setup. By a trial-and-error approach, a constant learning rate μ within the range of 0.025 and 0.04 is found sufficient for adequate stable convergence, which is consistent with Widrow-Hoff delta rule discussed in References [22, 23].

When mean-square error ε is minimized, the weight vector $\hat{W}$ after convergence would be

$$\hat{W} = [b_0,\ a_1,\ b_1,\ a_2,\ b_2, ..., a_{\mathrm{N}}, b_{\mathrm{N}}]^{\mathrm{T}}. \tag{42}$$

Thus the fundamental component of the measured signal $Y_1(t_{\mathrm{k}})$ is

$$Y_1(t_{\mathrm{k}}) = a_1 \sin\omega t_{\mathrm{k}} + b_1 \cos\omega t_{\mathrm{k}}. \tag{43}$$

Obviously, the dimension of the weight vector W_k to be updated depends on the order N of the harmonics to be estimated. In case of highly distorted load, lower order structure of neural network is not accurate enough when high convergence speed is required, so using higher order ANN structure is inevitable. However, higher order neural network results in heavy computational burden with poor performance in real-time harmonic compensation. Therefore, a synchronous frame ADALINE (SADALINE) is proposed to mitigate this problem.

It is well known that balanced nonlinear loads produce characteristic harmonics of the orders, -5, $+7$, -11, $+13 \ldots \pm 6n + 1$ (n is integer), corresponding to the $6n^{\text{th}}$ order harmonics in synchronous rotating frame due to one fundamental frequency shift from the stationary phase coordinate to synchronous rotating reference frame, as discussed in Reference [24]. Therefore, for harmonic estimation of three-phase rectifier load currents, only the weights for characteristic harmonics ($6n^{\text{th}}$ order) are needed to be updated in the synchronous frame ADALINE. With this simplification, the computational load is significantly reduced and the speed of weights iteration is greatly enhanced.

5.3. Voltage loop control. As shown in Fig. 5, the difference between the actual and the reference voltage is fed to the voltage loop controller. A separate proportional-integral (PI) controller is used to regulate *dc*-link voltage of the VSI in order to balance the active power flow, which can be expressed as

$$i_{\mathrm{fd}}^{*} = \left(k_{\mathrm{pdc}} + \frac{1}{s}k_{\mathrm{idc}}\right)(v_{\mathrm{dc}}^{\mathrm{ref}} - v_{\mathrm{dc}}), \tag{44}$$

where k_{pdc} and k_{idc} are proportional and integral gains of voltage loop controller, respectively, and $v_{\mathrm{dc}}^{\mathrm{ref}}$ is the reference voltage of the VSI *dc*-side capacitor. The output of this controller is finally fed into the d-axis current controller. In the steady state, the average *dc*-side voltage would be constant, thus the fundamental components of source side currents and load side currents are equal.

6. Experimental results

To verify the effectiveness of the proposed SADALINE algorithm for three-phase rectifier application, a laboratory prototype is established. The digital signal processor from Texas Instrument (TMS320LF2812) is selected as main controller for the system. And Cyclone Field Programmable Gate Array (FPGA) microchip is used to generate PWM waveforms for the IGBT (SKM200GB128DA) drivers. The system parameters are, $Z_{\mathrm{s}} = 0.02\ \Omega$, $L_1 = 0.53$ mH, $L_2 = 1.06$ mH, $L_5 = 3.824$ mH, $C_5 = 106\ \mu$F, $R_5 = 0.2$ ohm, VSI *dc*-side capacitor equals to 6800 μF. The parameters of control system are, $k_{\mathrm{pcc}} = 20$, $k_{\mathrm{icc}} = 300$, $k_{\mathrm{pdc}} = 3$ and $k_{\mathrm{idc}} = 15$. Various load conditions from 15 kW to 140 kW are tested, which are parallel connected with 10000 μF capacitor at the *dc*-side of diode rectifier. Besides, the EMI filter parameters are, $R_{\mathrm{EMI}} = 1.0\ \Omega$, $C_{\mathrm{EMI}} = 10\ \mu$F.

The performance of the SADALINE algorithm under different learning rate is presented in Fig. 6. The rectifier load is increased from 15 kW to 30 kW to test the dynamic performance of the weights updating process. It is found that

the learning rate (μ) has a significant effect on the performance of SADALINE. Figure 6 shows the simulation results regarding to the variation of SADALINE error, estimated fundamental current of the d-axis load current. The symbol T in the horizontal-axis represents one fundamental frequency period, corresponding to 200 sampling points. Here the d-axis component of the rectifier load currents is used as input of SADALINE to investigate the optimal learning rate for the weights updating process. The learning rate in Fig. 6a) is set to 0.015, and it can be observed that the transient response is very slow and the estimation error is high. When the learning rate is increased, the transient response becomes faster and the estimation error is reduced. Figure 6b) shows the optimal performance when the learning rate is set to 0.035. Higher learning rate as shown in Fig. 3c) ($\mu = 0.055$) results in excessive high overshoot in the estimated fundamental component, although the estimation error is reduced. It is found that the benchmark for tuning the learning rate is the dynamic performance of the weights updating process, not the estimation error of ADALINE. Theoretical analysis and experiments reveal that optimal performance can be achieved when the learning rate is in the range of 0.025 and 0.04.

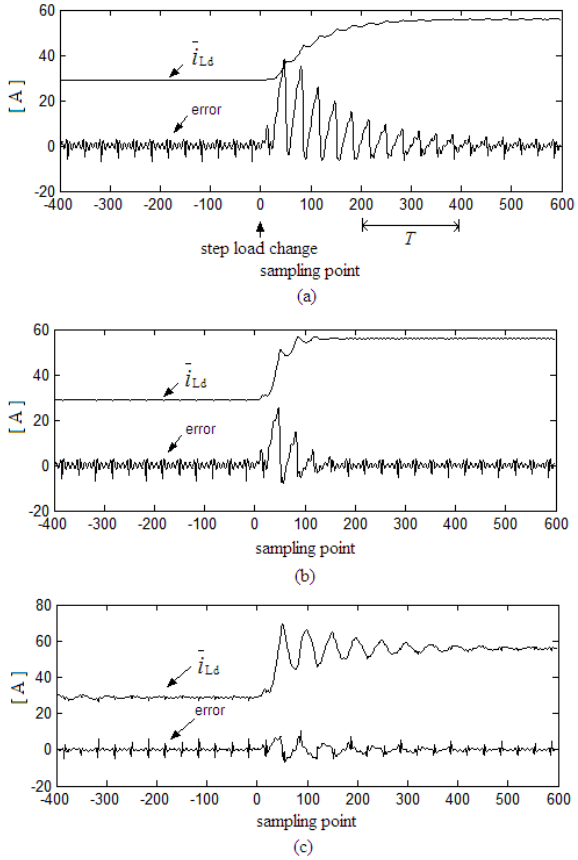

Fig. 6. Variation of SADALINE estimation error, estimated d-axis fundamental current with time, a) $\mu = 0.015$; b) $\mu = 0.035$; and c) $\mu = 0.055$

The harmonic orders considered in SADALINE are a trade-off between the required estimation accuracy and the available computational resources. When the proposed harmonic-free power factor corrector is used for improving power factor and harmonic elimination of 3-phase six-pulse bridge rectifier loads (front-end rectifier for *ac*-drive applications), characteristic harmonics (($6n\pm1$)$^{\text{th}}$ order, n is integer) are sufficient in the weights updating process. Figure 7 shows the simulation results when the different harmonic orders are considered in SADALINE for compensating the six-pulse rectifier load. Figure 7a) shows the case when only *dc* component is considered in SADALINE, it can be observed that the estimated fundamental components contain fluctuating ripples, and the estimation error of SADALINE is remarkable. Figure 7b) shows the case when *dc* component and the 6$^{\text{th}}$ order harmonics are considered in SADALINE, corresponding to the 5$^{\text{th}}$ and 7$^{\text{th}}$ order harmonics in stationary phase $a-b-c$ frame. Figure 7c) shows the case when *dc* component, the 6$^{\text{th}}$ and 12$^{\text{th}}$ order harmonics are considered in SADALINE. It is interesting to notice from Fig. 7c) that the estimated fundamental component is almost ripple-free. Therefore, it's proven that the required harmonic components to be considered in SADALINE algorithm can be noticeably reduced and higher order harmonics are not needed to be considered in the weights updating process. Hence the required computational resources required can be significantly diminished in the real-time implementation when the SADALINE algorithm is used for controlling the proposed harmonic-free PFC system.

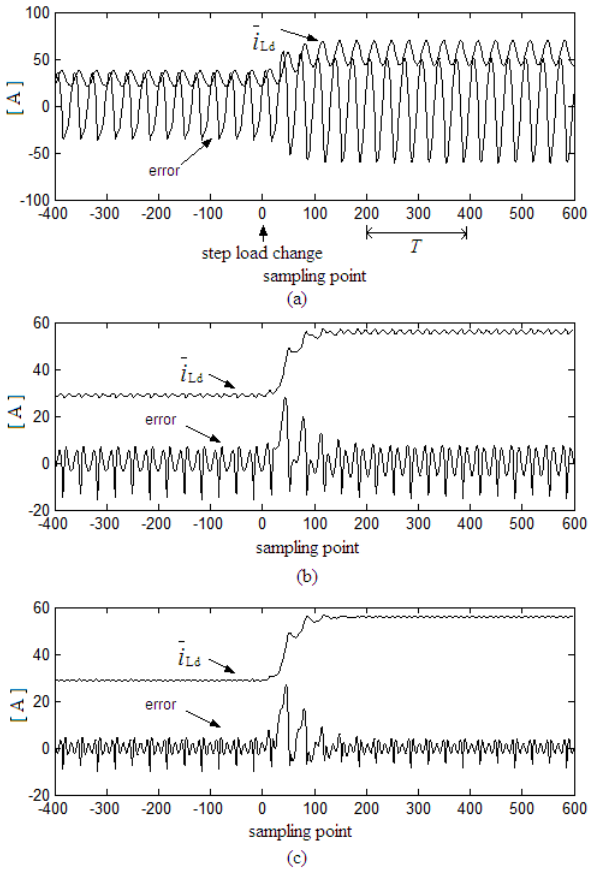

Fig. 7. Effect of harmonic order considered in SADALINE for the six-pulse rectifier load, a) only *dc* component is considered; b) *dc* component and 6$^{\text{th}}$ order harmonics are considered; and c) *dc* component, 6$^{\text{th}}$ and 12$^{\text{th}}$ order harmonics are considered

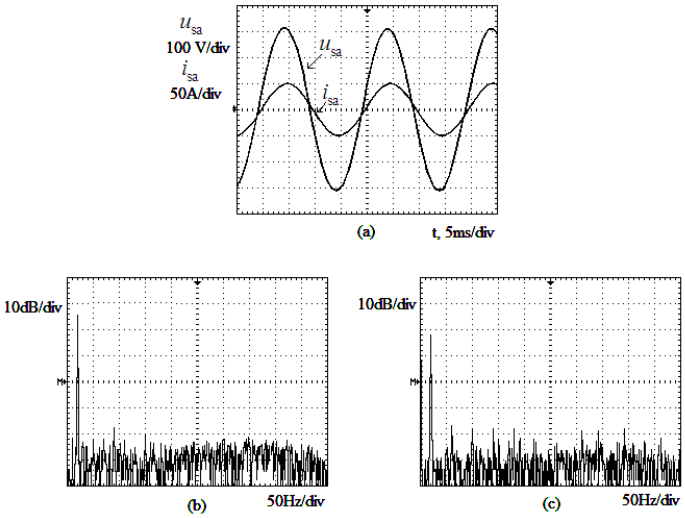

Fig. 8. Experimental results for steady-state operations, a) Source side voltage $u_{\rm sa}$ and current $i_{\rm sa}$; b) spectrum of $u_{\rm sa}$ and c) spectrum of $i_{\rm sa}$. The experimental waveforms were obtained after an analog low pass filter (LPF) before the probe of oscilloscope

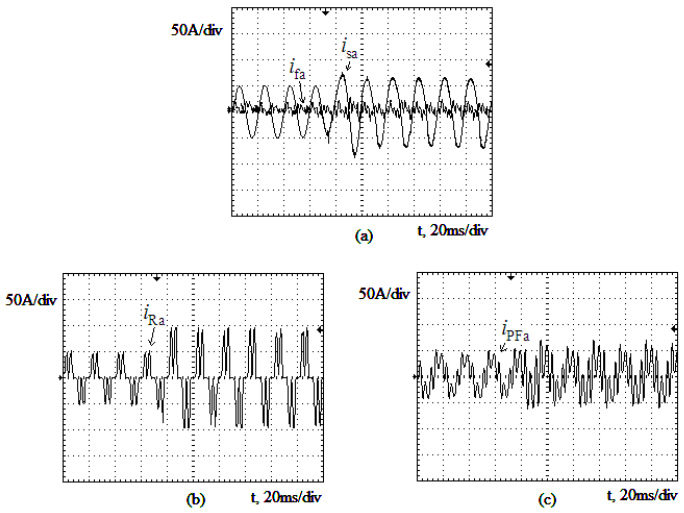

Fig. 9. Experimental results for transient response, a) source side current$i_{\rm sa}$, VSI compensating current $i_{\rm fa}$; b) rectifier current $i_{\rm Ra}$ and c) passive filter current $i_{\rm PF}$

Figure 8 shows the steady-state experimental results for the 15 kW rectifier load. Figure 8a) shows the source-side voltage and current, it shows that the source current is almost sine wave after compensation. Figures 8b) and c) show the spectrum of source-side voltage and current. The total harmonic distortion (THD) of grid voltage is less than 2%, and the THD of $i_{\rm sa}$ is about 4-5%. And the power factor at the source side is almost unity. Figure 9 shows the transient response when another 15kW resistive load is suddenly applied to the *dc*-side of the diode rectifier. Figure 9a) shows source side current $i_{\rm sa}$ and compensating current $i_{\rm fa}$. A low pass filter is applied to extract the current envelope from $i_{\rm fa}$, and it mainly contains $7^{\rm th}$ and $11^{\rm th}$ harmonic components since the dominant $5^{\rm th}$ order harmonic generated by the rectifier load has almost been eliminated by the passive filter. Figures 9b) and c) show the rectifier current $i_{\rm Ra}$ and the passive filter current $i_{\rm PF}$ of phase 'a', respectively. It can be observed that the passive filter shares a majority of load current, and the VSI current is much smaller compared with passive filter current. Besides, the transient process dies out in less than one fundamental cycle, which is consistent with the simulation results of the adaptive linear neural network (ADALINE).

Table 1 summarizes the measured total harmonic distortion (THD) of grid voltage in phase 'a' under different load conditions. The results of the following three scenarios are presented,

- Scenario one, Both the T-type APF and the passive filter are not connected;
- Scenario two, Only the passive filter is connected, and the T-type APF is not connected;
- Scenario three, Both the T-type APF and the passive filter are connected.

Table 1
Measured total harmonic distortion (THD) of grid voltage in phase 'a'

Rectifier load (kW)	Without APF and PF	Without APF, with PF	With APF and PF
15	2.45%	2.65%	1.96%
30	3.16%	3.38%	1.99%
50	4.45%	4.48%	2.08%
100	5.92%	5.75%	2.12%
140	7.65%	6.64%	2.26%

It can be seen from Table I that the THD of grid voltage is less than 5% when the load power is less than 50 kW, which is within the IEEE 519-1992 voltage distortion limits (5% THD in grid voltage for the distribution system with the bus voltage less than 69 kV) reported in References [25–28]. However, the IEEE 519-1992 voltage distortion limits are violated when the load power is increased to higher than 100 kW. Besides, the THD of grid voltage for scenario two is a little higher than the case for scenario one when the load is less than 50 kW, which is the typical harmonic amplification phenomenon caused by the passive filter under light load. This phenomenon of harmonic amplification under light load is also widespread in many electrical distribution substations with fixed reactive compensators or switching capacitors, as discussed in Reference [26]. Under this situation, the active power filter is a mandatory to suppress the unwanted harmonic amplification. Furthermore, the harmonic amplification phenomenon for scenario two no longer exists when the load power is increased to 100 kW and 140 kW. It also shows in Table 1 that the THDs of grid voltage for scenario three are significantly reduced compared with the first two scenarios. And the THDs of grid voltage for scenario three are strictly within the IEEE 519-1992 voltage distortion limits under all the load conditions.

Figure 10 shows measured individual harmonic distortion (IHD) of grid current $i_{\rm sa}$ and rectifier load current $i_{\rm Ra}$ in comparison with the IEEE 519-1992 current distortion limits [25–28] under different load conditions. And the IHD is defined as

$$IHD = \frac{I_{\rm n}}{I_{\rm f}} \times 100\%, \tag{45}$$

where $I_{\rm n}$ and $I_{\rm f}$ represent the amplitudes of the $n^{\rm th}$ order harmonic component and the fundamental component of the measured current, respectively.

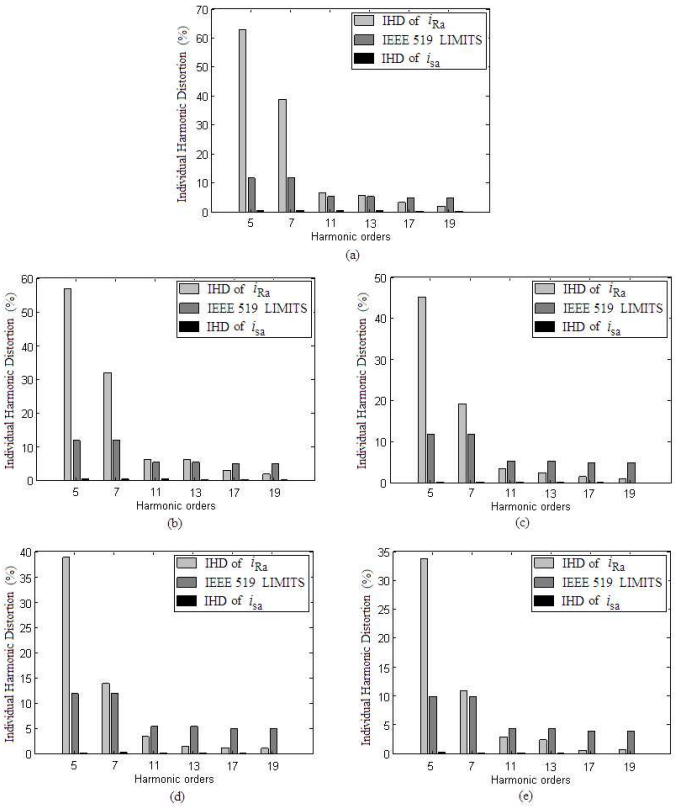

Fig. 10. Measured individual harmonic distortions (IHD) of the grid current $i_{\rm sa}$ and rectifier load current $i_{\rm Ra}$ in comparison with the IEEE 519-1992 current distortion limits, a) load power=15 kW; b) load power=30 kW; c) load power=50 kW; d) load power=100kW and e) load power=140 kW

Figures 10a) and b) show that the 5$^{\rm th}$, 7$^{\rm th}$, 11$^{\rm th}$ and 13$^{\rm th}$ order harmonics generated by the nonlinear rectifier load violates the IEEE 519-1992 current distortion limits when the load power equals to 15 kW and 30 kW. Figures 10c)–e) show that the 5$^{\rm th}$ and 7$^{\rm th}$ order harmonic components generated by the nonlinear rectifier load violate the IEEE 519-1992 current distortion limits when the load power equals to 50 kW, 100 kW and 140 kW. After the effective compensation of the proposed system, the IHDs of source side current $i_{\rm sa}$ are strictly within the IEEE 519-1992 current distortion limits under all the load conditions. Moreover, it is also found that the value of load current IHD decreases with the increase of load power since the fundamental component of load current increases more rapidly compared with the harmonic components.

Figure 11 shows the measured total harmonic distortion (THD) of the grid current $i_{\rm sa}$ and rectifier load current $i_{\rm Ra}$ in comparison with the IEEE 519-1992 current distortion limits under various load conditions. In Fig. 11, $I_{\rm SC}$ is specified as

$$I_{\rm SC} = \frac{S}{\sqrt{3}U \cdot Z_{\rm d}\%} \times 1000, \qquad (46)$$

where S is the capacity of distribution transformer (1000 kVA), U is the transformer secondary voltage (380 V), and $Z_{\rm d}\%$ is the short-circuit impedance of transformer (6%). And $I_{\rm L}$ is defined as the maximum demand load current measured at the PCC [25]. Hence the quantity $I_{\rm SC}/I_{\rm L}$ in the horizontal axis of Fig. 11 represents the ratio of the short-circuit current available at the point of common coupling (PCC), to the maximum fundamental load current. Therefore, as the size of the user load increases with respect to the size of the electrical distribution system, the percentage of harmonic current that the user is allowed to inject into the utility decreases. This philosophy of restricting the harmonic injection, as discussed in References [25–28], protects other users on the same feeder as well as the utility, which is required to furnish quality of voltage to its customers.

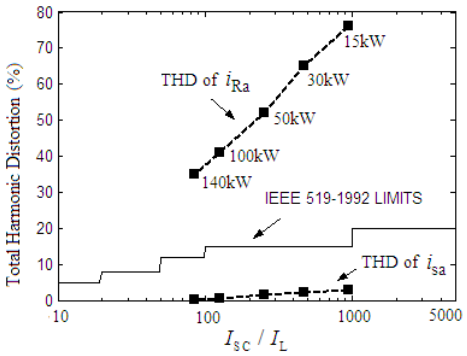

Fig. 11. Measured total harmonic distortions (THD) of the grid current $i_{\rm sa}$ and rectifier load current $i_{\rm Ra}$ in comparison with the IEEE 519-1992 current distortion limits under various load conditions

It shows, in Fig. 11, that the THD of rectifier current $i_{\rm Ra}$ violates the IEEE 519-1992 current distortion limits under all the tested load conditions, ranging from 15 kW to 140 kW. However, the THDs of source side current $i_{\rm sa}$ are strictly within the IEEE 519-1992 current distortion limits, which substantially verified the effectiveness of the proposed system.

7. Concluding remarks

In this study, we presented a novel three-phase harmonic-free power factor corrector topology based on T-type active power filter for power factor correction and harmonic compensation of six-pulse rectifier converter loads. The power rating of the voltage source inverter is significantly reduced by connecting passive filter in parallel with the T-type active power filter for fundamental reactive power compensation and harmonic attenuation of the dominant harmonics.

To guarantee compensation accuracy and dynamic performance under load transients, we presented a control strategy by using separate proportional integral (PI) controllers in d-axis and q-axis in current loop controllers to regulate real and reactive power, respectively. And load side disturbances are feed forwarded in the current loop controllers by using two groups of synchronous frame adaptive linear neural networks (SADALINEs). Besides, a separate proportional-integral controller is in the voltage loop for balancing the active power flow of the voltage source inverter.

Theoretical analysis and experimental results confirm well the effectiveness of the proposed system and its control scheme. The proposed harmonic-free PFC topology as well as its control scheme can find wide applications in the front-end rectifier of six-pulse converters, especially in *ac*-drive applications.

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