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Dedicated to Professor Wiesław Woliński
on the occasion of his eightieth birthday

Surface smoothness improvement of HgCdTe layers grown by MOCVD

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Abstract. This paper presents results of experimental efforts pointed towards morphology improvement of HgCdTe layers grown by MOCVD on GaAs substrates. Selected growth parameters on morphology state are presented. The substrate issues like its quality and crystallographic orientation have been discussed. Also influence of HgCdTe layer thickness on its surface roughness is described.

It is shown that extensive characterization studies using accessible equipments and methods: atomic force microscopy (AFM), secondary electron microscopy (SEM), laser scatterometer and Nomarski microscopy, have provided invaluable information about the correlation between defect formation and the influence of specific growth parameters.

Key words: HgCdTe MOCVD growth, layer morphology, surface smoothness.

1. Introduction

HgCdTe is still one of the key component of infrared sensing industry [1]. The market demand as well as other competitive technologies make higher requirements for improving the HgCdTe heterostructure parameters. Surface morphology reflects most bulk defects of the crystal structure of the sample and hence the correlation between layers surface morphology quality and photoelectrical parameters of devices made on the basis of these layers is obvious.

Although the lattice mismatch between CdTe and GaAs is about 14%, high quality single crystal layers with featureless morphology could be obtained and GaAs substrates.

Fabrication of high quality IR detector demands high levels of homogeneity of the material in terms of composition and defects, in addition to a good surface planarity of the epilayer surface. A good surface planarity of epilayers is also very important from the point of view of device processing.

Surface defects commonly observed on HgCdTe films include microtwins, dislocations, hillocks and voids, depending on the growth techniques and growth conditions [3]. Surface topography plays a vital role in determining yield limiting device fabrication processes as well as providing insight into growth optimization. Fine control over the defect density is necessary to improve device performance.

The decisive role in the surface state of HgCdTe layers play its crystallographic orientation [4, 5], hence we focused our attention for selecting the optimal growth orientation. We applied interdiffuse multilayer process (IMP) to grow HgCdTe layers [6], although other research centers still make efforts to improve alternative direct alloy growth (DAG) method [7, 8].

There are many factors which influence the quality of MOCVD deposited HgCdTe layers. Among those which can be optimized with respect to morphology, we can modify: substrate orientation/disorientation, substrate quality, nucleation conditions, growth temperature (substrate and Hg zone temperatures), prior to growth treatment, growth pressure, II/VI ratio, gas flow rates, IMP modification, buffer layer thickness, wafer rotation, and precursors partial pressures.

In the paper we report a study of the surface quality of HgCdTe layers deposited by MOCVD on GaAs substrates.

2. Experiment

HgCdTe layers were grown at atmospheric pressure in a horizontal vent-run type MOCVD reactor (AIX200 Aixtron built system). For this purpose, electronic grade diisopropyltelluride (DIPTe) and dimethylcadmium (DMCd) were used as Te and Cd precursors, respectively. Elemental mercury was used in quartz bath as Hg precursor. Two inches epiready GaAs wafers of different orientation were used as a substrates and H_2 was used as the carrier gas. The total H_2 flow rate through the reactor chamber was kept constant at 2400 sccm during CdTe growth. During HgTe IMP phase the H_2 flow rates were kept at 600 and 100 sccm in the upper (cadmium) and the lower (tellurium) parts of the reactor, respectively. Growth of MOCVD HgCdTe epilayers and their properties are described in details in previously published papers, e.g. in Refs. [9] and [10].

Thickness of CdTe buffer layers has been changed from 0.5-μm to 4-μm and HgCdTe layers – from single micrometers up to 30 μm. Samples were cleaved and their thickness was measured by optical microscope.

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2.1. Substrate issues. One of the most important factor decisive for HgCdTe/CdTe surface smoothness is the substrate quality [11]. Different types of substrates and different designs of buffer layers and theirs influence on HgCdTe heterostructures parameters are described in Ref. [12]. Final substrate preparation (etching, polishing and rinsing) is individual manufacturer's recipe of the epiready substrate.

The state of surface smoothness is the first criterion assessed for as grown layer. If it is uniform and shiny then is passed for measurements and processing, if is matt then points that something was wrong with the growth process or the substrate.

Figure 1 presents photos of 3-μm thick CdTe buffer layers on GaAs substrates from different suppliers. Each CdTe buffer layers is eye-estimated and even without microscope usage some of them (typically 20%) are disqualified for subsequent HgCdTe growth. Figure 1a) reflects traces remained after wrong final substrate preparation probably coming from final rinsing. This CdTe buffer is not suitable for further device preparation. On the contrary, Fig. 1b) presents mirror like CdTe buffer layer and this should be destined for subsequent HgCdTe heterostructure growth.

a)

b)

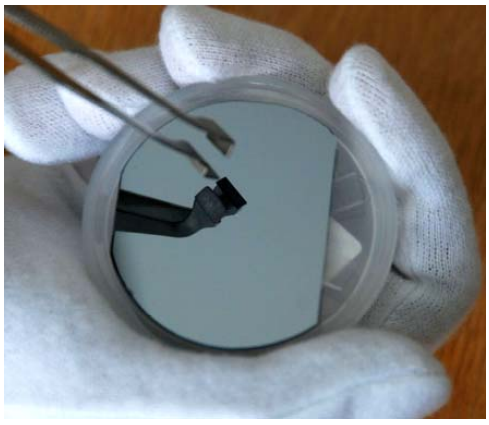


Fig. 1. Surface state of 3-μm thick CdTe buffer layers on GaAs substrates from different suppliers

Among wide spectrum of possible orientations we have focused our researches on GaAs(100) and GaAs(211)B substrate orientations. Our growth conditions leads to CdTe buffers with (100) or (111)B orientation on GaAs(100). The CdTe orientation is govern by sequence of precursor's switching. Introducing DMCd before DIPTe we obtain CdTe (100) orientation, instead (111)B orientation by introducing DIPTe before DMCd. Similar experiments have been already reported [13]. The investigation to these three types of HgCdTe orientations [(100), (111)B and (211)B] results from extensive literature study and necessity of finding the shortest way to achieve reproducible, device quality heterostructures.

The best smoothness we have observed on HgCdTe (100) layers, but those occurred only few times on substrates from a supplier who does not exist now. Vast majority of HgCdTe(100) were full of hillocks with height comparable to the layer thickness. More detailed description of our results with HgCdTe(100) structures has been published ealier [9]. There are some methods of reducing hillock density on HgCdTe(100) layers, e.g. by rinsing substrate with KOH water solution [14, 15], but out experiences did not give positive results in that way.

The CdTe(111)B surface morphology grown on GaAs(100) substrates is shown in Fig. 2. It presents irregular texture, which indicates on high density of screw defects. The surface mean roughness determined by AFM is 12 nm. This poor morphology may be related to the twinned growth that is characteristic of this orientation [16]. The growth mechanisms that rule the growth process of (111)CdTe on (100)GaAs substrates has been already described [17].

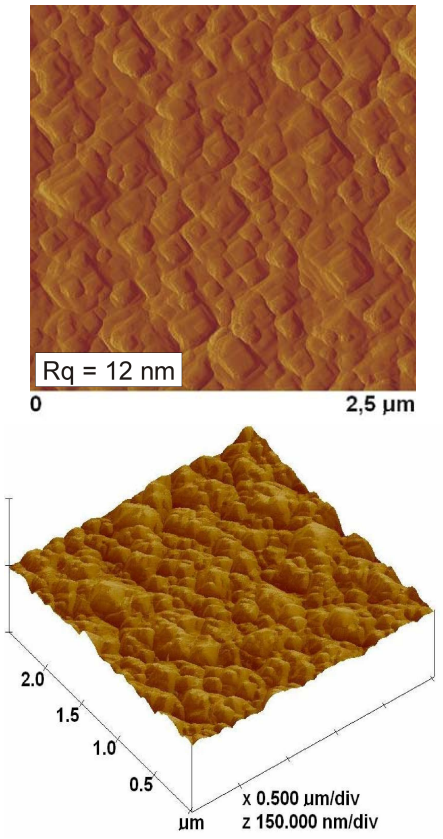


Fig. 2. Surface morphology of CdTe(111)B buffer on GaAs(100) substrate from Supplier 1 (process: #736)

In spite of rough surface topography of (111)CdTe buffers visible in Fig. 2, the 15-μm thick HgCdTe heterostructures with a surface roughness $\pm$ 80 nm can be grown with sufficient electrical parameters for IR devices fabrication [9]. Simultaneously, we have studied CdTe buffer layer growth with alternative crystallographic orientations.

Considerable morphology difference between CdTe layers of the same orientation (211)B, but coming from different supplier, are visible in Fig. 3. We do not know the exact reason of those differences. We can suspect that the reason resides in differences is growth methods. Substrates from Supplier 1 were grown by vertical gradient freeze (VGF) technique, but substrates from Supplier 2 were grown by liquid encapsulated Czochralski (LEC) technique. The etch pit density (EPD) value is about one order of magnitude better for VGF method. We can also suspect some differences in final surface substrate preparation or some differences in precise crystallographic orientation determination which influence on surface morphology.

The surface morphology of CdTe (211)B layer deposited on GaAs substrate from Supplier 1 is shown in Fig. 3a). It is characterized by elongated shapes resembling the sea waves. We are not sure about the reason of this type of roughness. The source of this type of unevenness probably results in lattice mismatch between CdTe and GaAs, the GaAs surface roughness, or in the lack of optimal CdTe growth conditions. Surface mean roughness is about 7 nm. The 10-μm thick HgCdTe layers grown on GaAs (211)B substrates from Supplier 1 with a surface roughness less than 50 nm fully meet device requirements and may be useful for device fabrication.

The surface morphology of CdTe (211)B layer deposited on GaAs substrate from Supplier 2 is shown in Fig. 3b). It is characterized by irregular and high density screw defects. The determined surface mean roughness is about 4 nm. This value is better in comparison with that obtained for Supplier 1 but the shape of irregularities is not convenient for heterostructures growth. The 10-μm thick HgCdTe layers grown on this type of substrate with surface roughness more than 100 nm are not suitable for device fabrication and we cease researches with GaAs substrates from Supplier 2.

For characterization CdTe buffer layers we also use optical microscope with Nomarski contrast. As we can see in Fig. 4, decisive role for surface morphology of CdTe buffer layer plays not only GaAs substrate orientation but also their direction of disorientation. Changing disorientation direction from [110]A to [111]A the surface roughness was improved from 81 nm to 72 nm. However, the value of 72 nm is still far from desirable smoothness of CdTe buffer layer. Here, we could present only two from huge amount of possible disorientation directions. Reasonable experiments focused on surface smoothness improvement should research the best disorientation direction – for surface smoothness optimization however this meets economical barrier. Potential benefit to cost ratio together with risk probability calculation should be considered in this case particularly.

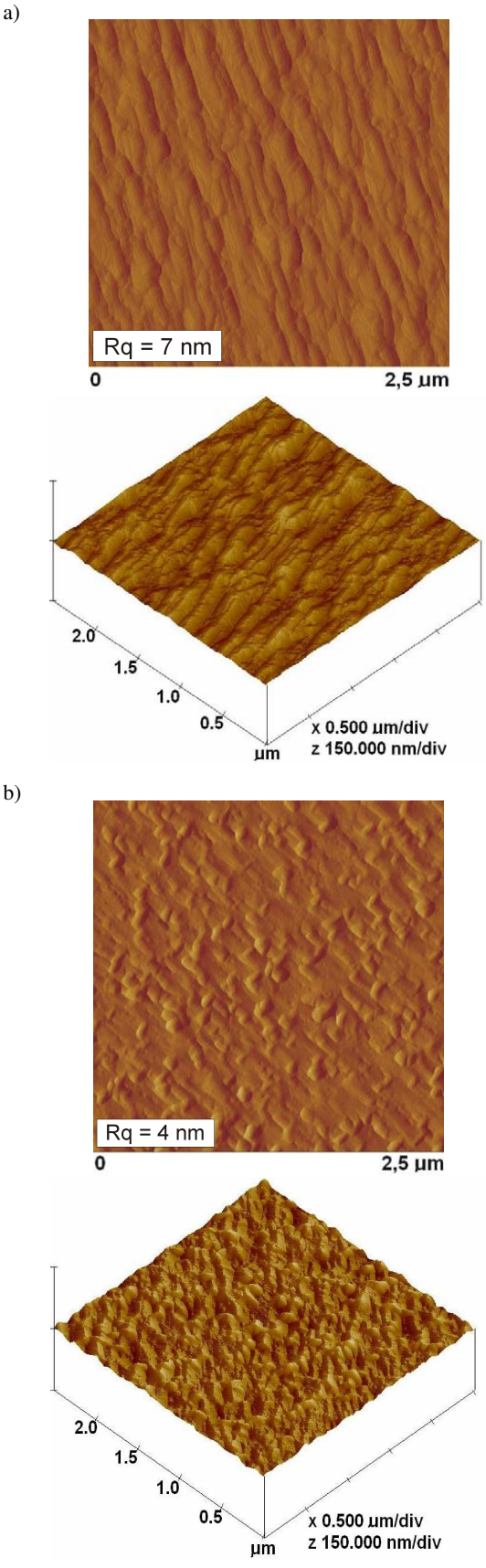


Fig. 3. Surface morphology of CdTe(211)B buffers on GaAs(211)B substrates from Supplier 1 – process #740 a) and Supplier 2 – process #701 b)

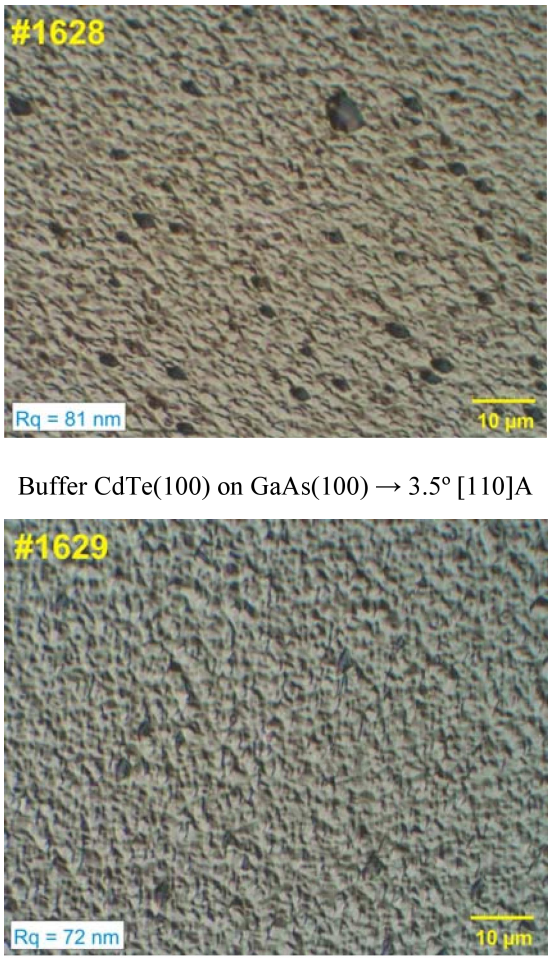


Fig. 4. Surface morphology of buffer CdTe(100) 2-μm thick buffer layers on GaAs(100) substrates with different directions of disorientations

2.2. Experiments with MBE/MOCVD buffer layers. Because of unsuccessful experiments with deposition of hillock-free HgCdTe(100) layers, we decided to check if the problem reside in nucleation conditions or in growth conditions. We have intended to test surface morphology using alternative to MOCVD growth method. Increasing number of reports presenting high quality and mirror like HgCdTe(100) heterostructures fabricated by MBE [18–20] inclined us to deposit several CdTe buffers by this method. These CdTe buffer layers were deposited by MBE system in Institute of Physics Polish Academy of Science, Warsaw. In the next steps the MOCVD HgCdTe epilayers on MBE CdTe buffers have been deposited.

The MOVPE/MBE combination using the advantages of both techniques has already been performed [18]. Ultra high vacuum (UHV) has been used for pretreatment of the GaAs substrate and CdTe buffer layer, while the volatile mercury used in the HgCdTe growth was handled at atmospheric pressure in the MOVPE system, thus avoiding the problem of trying to maintain UHV in the presence of mercury.

The surface morphology of 3-μm and 0.5-μm thick CdTe buffer layers on GaAs substrates deposited by MBE are presented in Fig. 5. The pictures were made using 1000× optical microscope with Nomarski contrast. On both photos there are a lot of visible defects, which can be divided for two groups. One group are defects originated from dust which appealed most probably before the growth process. These defects are as if blended into growing layer and are characterized by gentle (not sharp) shape. Second group of defects are hillocks. They are characterized by regular, sharp shape (their characteristic, pyramidal shape is better visible directly through microscope ocular during fluent microscope focusing).

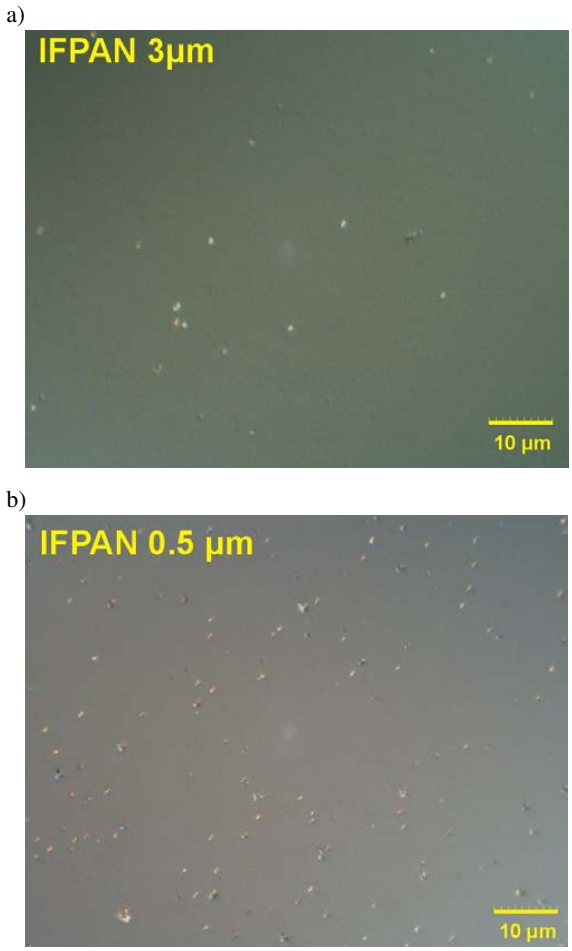
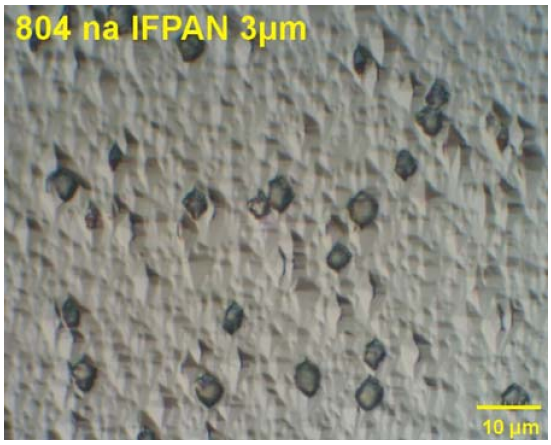


Fig. 5. Surface morphology of CdTe buffer layers grown by MBE on GaAs(100) substrates. Thickness of buffer layers: a) 3 μm, b) 0.5 μm

The surface morphology of 4.5-μm thick HgCdTe layer deposited by MOCVD on 3-μm and 0.5-μm thick CdTe buffer layers deposited by MBE are presented in Fig. 6. Both surfaces are dominated by high density of hillocks: that presented in Fig. 6a) has about 5×10^3 hillocks/mm^2, and that presented on Fig. 6b) has about 2×10^3 hillocks/mm^2. These defects are simply expanded defects initially seen on CdTe buffer layers and as consequence give negative result to subsequent HgCdTe heterostructure fabrication. Moreover, the HgCdTe layers grown on the CdTe buffers are characterized by decreased growth velocity probably because of lack of high temperature annealing before growth. Thus surface oxidants contribute in deterioration of HgCdTe growth process.

a)



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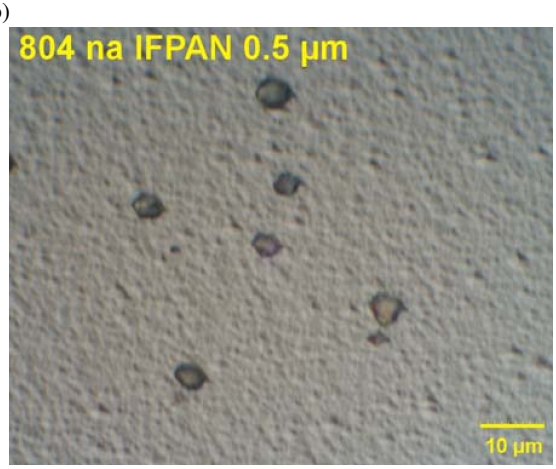
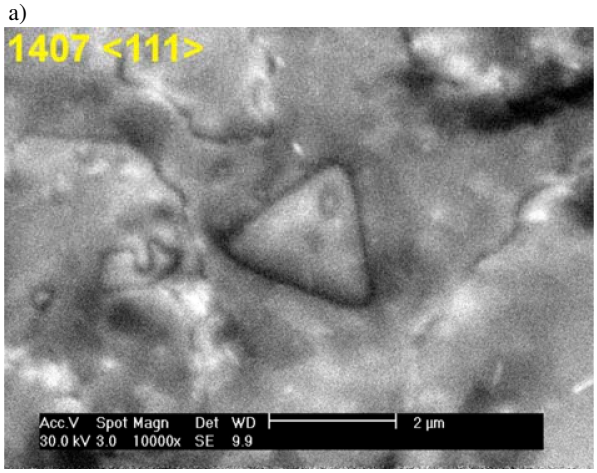


Fig. 6. Surface morphology of 4.5-μm thick MOCVD HgCdTe layers grown on MBE CdTe layers with thicknesses 3 μm a) and 0.5 μm b) on GaAs(100) substrates

a)



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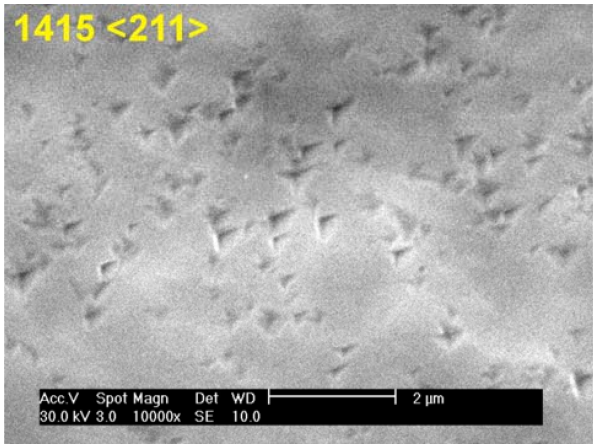


Fig. 7. SEM surface morphology of HgCdTe layers with different crystallographic orientations: a) 5-μm thick (111)HgCdTe layer on 2.5-μm thick CdTe buffer, b) 7-μm thick (211)HgCdTe layer on 2.5-μm thick CdTe buffer

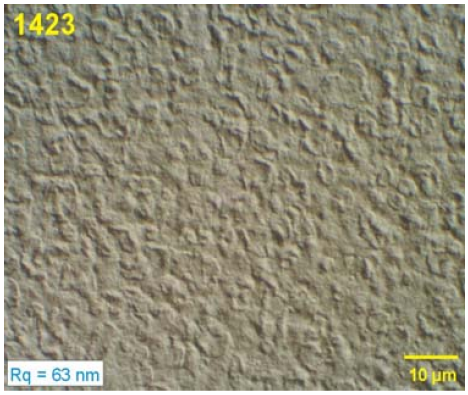
2.3. Optimization of HgCdTe growth process. Apart crucial role of the GaAs substrate quality also other important factors influencing on final HgCdTe morphology surface can be found in heterostructure growth details. For example, Fig. 7a) presents secondary electron microscopy (SEM) morphology of 5-μm thick HgCdTe(111) layer on 2.5-μm thick CdTe buffer layer. Surface morphology presents some single regular triangles characteristic of $<111>$ crystallographic orientation as well as many irregular shapes, which contributes to poor smoothness (Rq = 76 nm). Parameter Rq has been determined by total integrated scattering (TIS) method [21–23] using laser scatterometer type SL 31 produced by Polish Institute of Mathematical Machines, Warsaw [23]. The Rq parameter is the value of mean square deviation of surface roughness profile. Thus, the Rq parameter does not characterize the type or shape of surface defects but provides comparable data of smoothness of measured set of samples.

The SEM surface morphology of 7-μm thick HgCdTe(211) layer on 2.5-μm thick CdTe buffer layer is presented in Fig. 7b). Surface is determined by high density of different size triangles distributed without any regular patterns. The mean roughness Rq is about 45 nm.

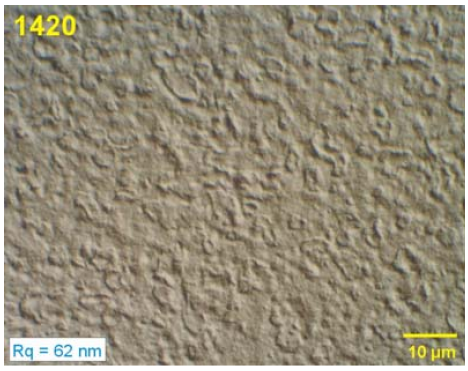
Next figure (Fig. 8) presents surface morphology of p-P$^+$ HgCdTe heterostructures grown at different temperatures with total thickness of 4 μm. The substrate temperature changes within the range of few degrees do not influence considerably on the surface state, but plays decisive role for HgCdTe composition. Within the range of applied growth temperatures, 343–360°C, the value of surface roughness oscillates near 65 nm and roughness deviations do not exceed measurement uncertainty (Fig. 9). Mercury zone temperature was kept constant at $T_{Hg} = 220$°C during this experiments.

The mercury temperature is measured by thermocouple placed within mercury bath through double quartz pipe. Such mercury temperature measurement conditions are not stable because of lack of precise and repeatable thermocouple placement especially that mercury bath is moved almost each time with the growth run. The mercury temperature changes within few degrees influence considerably on the HgCdTe layer composition. However, the mercury temperature changes as well as substrate temperature changes within few degrees do not influence considerably on the surface morphology quality as it was observed for the growth temperature changing.

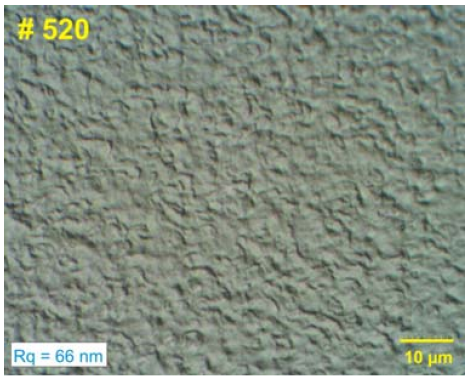
T_{gr} = 345ºC



T_{gr} = 349ºC



T_{gr} = 350ºC



T_{gr} = 360ºC

Fig. 8. Surface morphology of HgCdTe layers for different growth temperatures

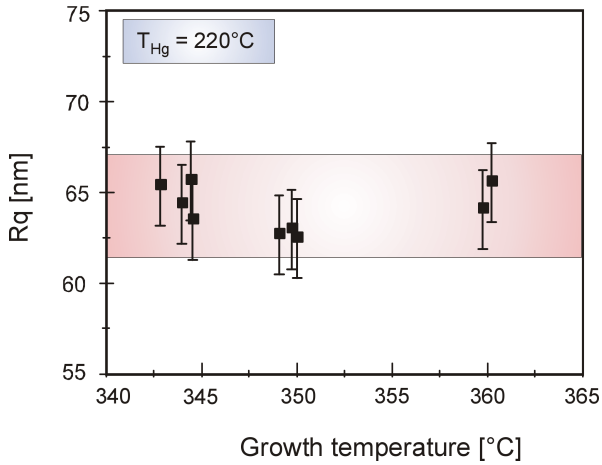


Fig. 9. Surface roughness, Rq, as a function of HgCdTe growth temperature

In parallel to growth temperature optimization (both substrate and Hg zone temperatures) we have carried out other experiments to obtain the best surface morphology. Table 1 presents important growth parameters optimized with respect to surface state.

Table 1
Selected growth parameters

Prior to growth treatment	380°C/15 min			
Nucleation condition	Cd flush for (100) growth orientation Te flush for (111) growth orientation			
Growth pressure	500 mbar			
Susceptor temperature	350°C			
Mercury zone temperature	210–220°C			
II/VI ratio	1.5–5 during CdTe cycles			
Wafer rotation	50 sccm			
Buffer layer thickness	3–5μm			
H_2 gas flow rates	HgTe	reactor gas artery	upper	600 sccm
			lower	100–200 sccm
	CdTe	reactor gas artery	upper	1200 sccm
			lower	1200 sccm

The growth parameters listed in Table 1 have been checked within providing range of the MOCVD system and within the range of HgCdTe physical growth conditions. The IMP modification growth process by precise determining the delay of precursors transport in H_2 machine gas system also contributed to morphology improvement. Detailed description of IMP growth process modification was described elsewhere [24].

Also the influence of thickness of HgCdTe layer on the surface roughness has been examined. Surface roughness, Rq, as a function of HgCdTe layer thickness for different crystallographic orientations is presented on Fig. 10. Surface roughness increase with structure thickness in approximately logarithmic way. The defects created at GaAs/CdTe interface and within the buffer layer are enhanced with the HgCdTe layer growth. The Rq parameter for <211>B orientation is approximately two times smaller than for HgCdTe layers with <111>B orientation. In spite of relatively good

surface smoothness of HgCdTe layers with <211>B orientation, our experiments were suspended due to the lack of progress in improvement device parameters fabricated on the basis of heterostructures with this orientation.

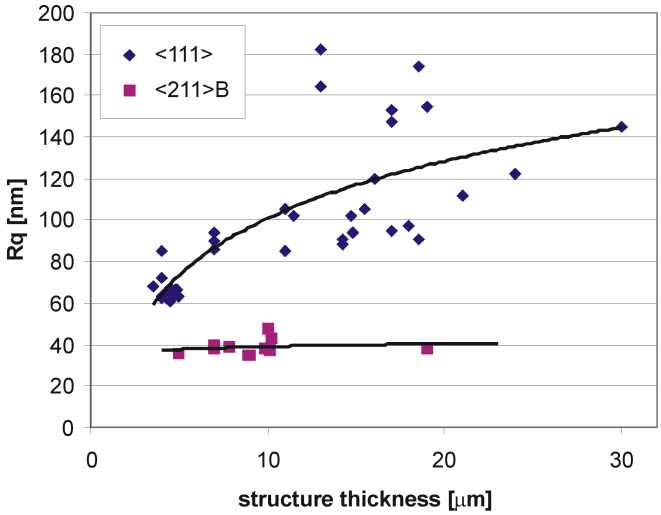


Fig. 10. Surface roughness, Rq, as a function of HgCdTe layer thickness for different crystallographic orientations

Finally, the roughness uniformity of HgCdTe layers across the whole area of the 2" wafer was examined. Figure 11 presents the surface roughness, Rq, as a function of the distance from the wafer center for different HgCdTe layer thickness. The surface roughness increases with (111)HgCdTe layer thickness. The smoothness uniformity varies up to 10% within whole wafer area and may be related not only with growth kinetics itself but may be related also with substrate surface preparation.

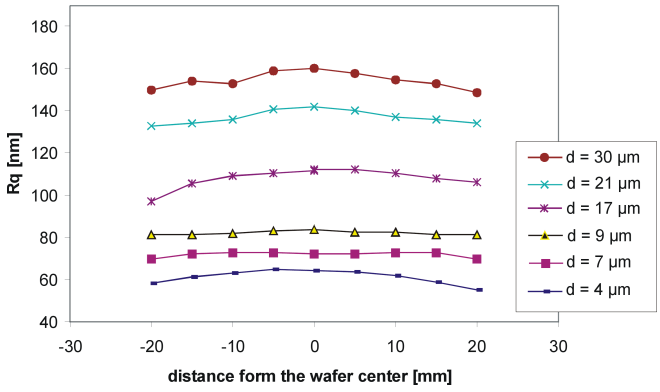


Fig. 11. Surface roughness, Rq, as a function of the distance from the wafer center for different (111)HgCdTe layer thickness

3. Summary

One of the crucial stages of MOCVD HgCdTe epitaxy is CdTe nucleation on GaAs substrate. Composite substrates have been obtained with suitable substrate preparation, liner and susceptor treatment, proper control of background fluxes and appropriate nucleation conditions [10]. Due to the large mismatch between GaAs and CdTe, both (100) and (111) growth may occur. It mostly depends on substrate disorientation and preparation, nucleation conditions and growth temperature. The GaAs/CdTe lattice mismatch is partially reduced by growth of 3–5-μm CdTe buffer layer. The growth of thicker CdTe buffers do not result in improving HgCdTe layers morphology in unambiguous way but enlarge heterostructure deposition time and cost.

We have pointed particular importance of GaAs substrate quality and its decisive role for HgCdTe heterostructure morphology smoothness. Substrate issues like its orientation, disorientation and final epiready preparation by supplier play the key role for HgCdTe surface roughness. Among several factors regarding the HgCdTe growth process, we restricted our investigations to the growth temperature, mercury zone temperature, HgCdTe layer thickness and its crystallographic orientation.

It is shown that the layer surface roughness increase with thickness of structure. The defects created at GaAs/CdTe interface and within the buffer layer are enhanced with the HgCdTe layer growth. The surface roughness parameter for <211>B orientation is approximately two times smaller than for HgCdTe layers with <111>B orientation. In spite of relatively good surface smoothness of HgCdTe layers with <211>B orientation, our experiments were suspended due to the lack of progress in improvement device parameters fabricated on the basis of heterostructures with this orientation.

In the paper selected results of our experiments focused on surface morphology improvement of CdTe as well as HgCdTe layers grown on GaAs substrates are reported. Interesting researches concerning correlation between the surface morphology and crystallographic structure of the material are the matter of huge concern of authors of this work. X-ray as well as TEM microscopy measurements of MOCVD grown HgCdTe heterostructures are currently performed in Institute of Physics Polish Academy of Science which will provide invaluable information about volume structure of the material and show the type of surface defects dependence on bulk structure defects. Such results will be the subject of the next paper of our team.

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REFERENCES

[1] A. Rogalski, "HgCdTe infrared detector material: history, status and outlook", *Rep. Prog. Phys*. 68, 2267–2336 (2005).

[2] S.K. Ghandhi, I.B. Bhat, and N.R. Taskar, "Growth and properties of $Hg_{1-x}Cd_xTe$ on GaAs substrates by organometalic vapor-phase epitaxy", *J. Appl. Phys*. 59, 2253–2255 (1986).

[3] L.H. Zhang, and C.J. Summers, "A study of void defects in metalorganic molecular-beam epitaxy grown HgCdTe", *J. Electron. Mater.* 27, 634–639 (1998).

[4] G. Cinader, A. Raizman, and A. Sher, "The effect of growth orientation on the morphology, composition, and growth rate of mercury cadmium telluride layers grown by metalorganic

vapor phase epitaxy", *J. Vac. Sci. Technol*. B9, 1634–1638 (1991).

[5] L.A. Almeida, M. Groenert, J. Markunas, and J.H. Dinan, "Influence of substrate orientation on the growth of HgCdTe by molecular beam epitaxy", *J. Electron. Mater.* 35, 1214–1218 (2006).

[6] S.J.C. Irvine, "Metal-organic vapour phase epitaxy" in *Narrow-gap II-VI Compounds for Optoelectronic and Electromagnetic Applications*, ed. P. Capper, pp. 71–96, Chapman & Hall, London, 1997.

[7] H. Nishino, S. Murakami, T. Saito, Y. Nishijima, and H. Takigawa, "Dislocation profiles in HgCdTe(100) on GaAs(100) grown by metalorganic chemical vapor deposition", *J. Electron. Mater.* 24, 533–537 (1995).

[8] H. Nishino, S. Murakami, and Y. Nishijima, "Structure and surface properties of metalorganic vapor phase epitaxial CdTe and HgCdTe(111)B layers grown on vicinal GaAs(100) substrates", *Jpn. J. Appl. Phys.* 38, 5775–5782 (1999).

[9] A. Piotrowski, P. Madejczyk, W. Gawron, K. Kłos, M. Romanis, M. Grudzień, J. Piotrowski, and A. Rogalski, „MOCVD growth of $Hg_{1-x}Cd_xTe$ heterostructures for uncooled infrared photodetectors", *Opto-Electron. Rev.* 14, 453–458 (2004).

[10] P. Madejczyk, A. Piotrowski, W. Gawron, K. Kłos, J. Pawluczyk, J. Rutkowski, J. Piotrowski, and A. Rogalski, "Growth and properties of MOCVD HgCdTe epilayers on GaAs substrate", *Opto-Electron. Rev.* 13, 239–251 (2005).

[11] R. Triboulet, A. Tromson-Carli, D. Lorans, and T. Nguyen Duy, "Substrate issues for the growth of mercury cadmium telluride", *J. Electron. Mater.* 22, 827–834 (1993).

[12] C.D. Maxey, J.C. Fitzmaurice, H.W. Lau, L.G. Hipwood, C.S. Shaw, C.L. Jones, and P. Capper, "Current status of large-area MOVPE growth of HgCdTe device heterostructures for infrared focal plane arrays", *J. Electron. Mater.* 35, 1275–1282 (2007).

[13] W.-S. Wang and I. Bhat, "(100) or (111) heteroepitaxy of CdTe layers on (100) GaAs substrates by organometallic vapor phase epitaxy", *Materials Chemistry and Physics* 51, 178–181 (1997).

[14] J.-S. Kim, Y.-H. Kim, B.-K. Kim, and H.-J. Je, "The role of surface adsorbates on electrical properties of MOVPE grown HgCdTe onto (001) GaAs substrats", *Solid-State Electronics* 48, 1623–1627 (2004).

[15] S.-H. Suh, J.H. Song, S.W. Moon, "Metalorganic vapor phase epitaxial growth of hillock free (100) HgCdTe/GaAs with good electrical properties, *J. Crystal Growth* 159, 1132–1135 (1996).

[16] I. Mora-Seró, C. Polop, C. Ocal, M. Aguiló, and V. Muñoz-Sanjosé, "Influence of twinned structure on the morphology of CdTe(111) layers grown by MOCVD on GaAs(100) substrates", *J. Crystal Growth* 257, 60–68 (2003).

[17] R.D. Feldman, D.W. Kisker, R.F. Austin, K.S. Jefers, and P.M. Bridenbaugh, "A comparison of CdTe grown on GaAs by molecular beam and organometallic vapor phase epitaxy", *J. Vac. Sci. Technol*. A4, 2234–2238 (1986).

[18] J.E. Halis, A.M. Keir, A. Graham, G.M. Williams, and J. Giess, "Influence of the silicon substrate on defect formation in MCT grown on II-VI buffered Si using a combined molecular beam epitaxy/metal organic vapor phase epitaxy technique", *J. Electron. Mater.* 36, 864–870 (2007).

[19] J.M. Peterson, J.A. Franklin, M. Reddy, S.M. Johnson, E. Smith, W.A. Radford, and I. Kasai, "High-quality large-area MBE HgCdTe/Si", *J. Electron. Mater.* 35, 1283–1286 (2006).

[20] P. Tribolet, S. Blondel, P. Costa, A. Combetee, L. Vial, G. Destefanis, P. Ballet, J.P. Zanatta, O. Gravrand, Ch. Largeron, J.P. Chamonal, and A. Millon, "MWIR focal planes arrays made with HgCdTe grown by MBE on germanium substrates", *Proc. SPIE* 6206, 62062F (2006).

[21] G.Y. Tian, R.S. Lu, and D. Gledhill, "Surface measurement using active vision and light scattering", *Optics and Lasers in Engineering* 45, 131–139 (2007).

[22] J. Lorincik and J. Fine, "Focusing properties of hemispherical mirrors for total integrating scattering instruments", *Applied Optics* 36, 8270–8274 (1997).

[23] *Laser Scatterometer SL* 31. *Manual – calibration*, Polish Institute of Mathematical Machines, Warsaw, www.imm.org.pl

[24] A. Piotrowski and K. Kłos, "Metal-organic chemical vapor deposition of $Hg_{1-x}Cd_xTe$ fully doped heterostructures without postgrowth anneal for uncooled MWIR and LWIR detectors", *J. Electron. Mater.* 36, 1052–1058 (2007).