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Tracing temperature characteristics in diode-transistor circuits having multiple DC solutions

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Abstract. The paper deals with circuits, composed of bipolar transistors, diodes, resistors and independent voltage sources, having multiple DC solutions. An algorithm for tracing temperature characteristics, expressing the output signal in terms of the chip temperature, is developed. It is based on the efficient method for finding all the DC solutions sketched in this paper. The algorithm gives complete characteristics which are multivalued and usually composed of disconnected branches. On the other hand the characteristics provided by SPICE are fragmentary, lose some branches or exhibit apparent hysteresis.

Key words: bipolar transistors, multiple DC solutions, temperature characteristics.

1. Introduction

Many nonlinear dynamic circuits, driven by DC sources, have multiple equilibrium points, which can be reached at different initial states. To determine the equilibrium points we short circuit all the inductors and open circuit all the capacitors, obtaining a resistive circuit. The equilibrium points are the DC solutions (operating points) of this circuit. Finding efficiently all the solutions is a difficult and still open question. In the past two decades numerous results have been derived, mainly based on piecewise-linear approximation, e.g. [1]-[6]. Unfortunately, only a few methods can be applied to circuits described by original nonlinear equations, e.g. [7]-[11]. They are able to analyze rather small-scale circuits.

This paper offers a method for finding all the DC solutions of diode-transistor circuits, without any piecewise-linear approximation. It improves some earlier ideas and employs new procedures. The method has a key role in the proposed algorithm for computing characteristics which express an output signal y (voltage or current) in terms of temperature T, $y = F(T)$. The characteristics of diode-transistor circuits having multiple DC solutions are multivalued and usually composed of disconnected branches. Using the approach developed in this paper the complete characteristics are computed under the assumption that all elements of the chip are at the same temperature, which varies in a prescribed range $[T^-, T^+]$. On the other hand the characteristics provided by PSPICE are fragmentary, lose some branches or exhibit apparent hysteresis.

Let us consider a chip containing linear resistors, diodes and bipolar transistors, driven by DC voltage sources. The transistors are represented by the Ebers-Moll model with the parameters depending on temperature T. Also small resistors R_E, R_C, R_B are included in the model.

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At any fixed temperature $T \in [T^-, T^+]$ the circuit can be described by the Sandberg-Willson equation [12]

$$\Gamma(T) f(v, T) + \boldsymbol{G}(T)\, \boldsymbol{v} - \boldsymbol{h}(T) = 0, \tag{1}$$

where $\boldsymbol{v} = \left[v_1 \cdots v_n\right]^{\mathrm{T}}$ is a vector of BE and BC voltages of the transistors and voltages across the individual diodes; $f(v,T) = \left[f_1(v_1,T) \cdots f_n(v_n,T)\right]^{\mathrm{T}}$, where $f_j(v_j, T)$, are the currents flowing through all the BE and BC diodes included in the Ebers-Moll model and the individual diodes. The currents are specified by the equations [13]:

$$i_{BE} = I_{SE}(T)\left(\mathrm{e}^{\lambda(T)v_{BE}} - 1\right),$$

$$i_{BC} = I_{SC}(T)\left(\mathrm{e}^{\lambda(T)v_{BC}} - 1\right),$$

$$i_D = I_{SD}(T)\left(\mathrm{e}^{\lambda(T)v_D} - 1\right),$$

where:

$$I_{SE}(T) = \frac{1}{\alpha_F(T)} I_0 \left(\frac{T}{T_0}\right)^{T_i} \exp\left(\frac{qE_g(T - T_0)}{kTT_0}\right),$$

$$I_{SC}(T) = \frac{1}{\alpha_R(T)} I_0 \left(\frac{T}{T_0}\right)^{T_i} \exp\left(\frac{qE_g(T - T_0)}{kTT_0}\right),$$

$$I_{SD}(T) = I_0 \left(\frac{T}{T_0}\right)^{\frac{T_i}{\eta}} \exp\left(\frac{qE_g(T - T_0)}{\eta kTT_0}\right),$$

$$\lambda(T) = \frac{q}{kT}.$$

In the above equations

In the above equations T_0 is the nominal temperature (300 K), I_0 is the saturation current at the nominal temperature, η is the emission coefficient, q is the electron charge, E_g is the energy gap, T_i is the saturation current temperature exponent,

$$\alpha_F(T)=\frac{\beta_{F_0}\left(\frac{T}{T_0}\right)^{T_\beta}}{\beta_{F_0}\left(\frac{T}{T_0}\right)^{T_\beta}+1},\quad \alpha_R(T)=\frac{\beta_{R_0}\left(\frac{T}{T_0}\right)^{T_\beta}}{\beta_{R_0}\left(\frac{T}{T_0}\right)^{T_\beta}+1},$$

where T_β is the user-supplied model parameter, β_{F_0} is the ideal maximum forward beta at T_0, β_{R_0} is the ideal maximum reverse beta at T_0.

$\boldsymbol{\Gamma}(T)$ is a block-diagonal matrix composed of the blocks

$$\begin{bmatrix} 1 & -\alpha_R(T) \\ -\alpha_F(T) & 1 \end{bmatrix}$$

corresponding to the transistors and the unit submatrix corresponding to the individual diodes, $\boldsymbol{G}(T)=\left[G_{ij}(T)\right]_{n\times n}$ is the admittance matrix and $\boldsymbol{h}(T)=\left[h_1(T)\dots h_n(T)\right]^{\mathrm{T}}$ is the source vector of a linear n-port created after extracting from the circuit all the transistors and diodes. The elements of matrix $\boldsymbol{G}(T)$ depend on the linear resistors, whereas the components of vector $\boldsymbol{h}(T)$ depend on the linear resistors and voltage sources. The resistances of the linear resistors inside the chip are temperature varying according to the equation

$$R(T)=R_0\left(1+T_{C_1}(T-T_0)+T_{C_2}(T-T_0)^2\right)$$

where R_o is the resistance at T_o, T_{c_1} (T_{c_2}) is the first order (second order) temperature coefficient.

Since $\boldsymbol{\Gamma}(T)$ is nonsingular matrix, Eq. (1) can be rearranged as follows

$$\boldsymbol{f}(\boldsymbol{v},T)+\boldsymbol{A}(T)\boldsymbol{v}-\boldsymbol{b}(T)=\boldsymbol{0} \tag{2}$$

where $\boldsymbol{A}(T)=\left[\boldsymbol{\Gamma}(T)\right]^{-1}\boldsymbol{G}(T)$, $\boldsymbol{b}(T)=\left[\boldsymbol{\Gamma}(T)\right]^{-1}\boldsymbol{h}(T)$.

To trace temperature characteristic $y=F(T)$ for $T\in\left[T^-,T^+\right]$, where y is an output signal (a voltage or current), we write equation expressing the output signal in terms of voltages $v_1,\dots,v_n$ and the voltage sources acting in the circuit

$$y=\sum_{j=1}^{n}h_j v_j+h_0 \tag{3}$$

and apply the algorithm sketched in Section 2. Since we analyze circuits having multiple DC solutions, the temperature characteristics are multivalued and usually composed of disconnected branches.

2. Tracing temperature characteristics

A crucial point of the algorithm for tracing temperature characteristics proposed in this section is based on a method for finding all the DC solutions at a fixed temperature. The method is used for computing all the solutions at $T=T^-$ They enable us to find the initial points of the characteristic branches using (3). Next we compute the subsequent points of each of the branches increasing the temperature by a small increment ΔT and solving equation (1) applying the Newton-Raphson algorithm. An appropriate procedure has been developed to overcome the turning-point problem. To guarantee finding all the branches we compute additionally all the solutions at $T=T^+$ and, if it is necessary trace some branches of the characteristic starting with these solutions and decreasing temperature.

Thus, a key point of the algorithm is a method for finding all the DC solutions at a fixed temperature. In such a case equation (2), describing the circuit, reduces to

$$\boldsymbol{f}(\boldsymbol{v})+\boldsymbol{A}\boldsymbol{v}-\boldsymbol{b}=\boldsymbol{0} \tag{4}$$

where $\boldsymbol{v}=\left[v_1\cdots v_n\right]^{\mathrm{T}}$, $\boldsymbol{b}=\left[b_1\cdots b_n\right]^{\mathrm{T}}$, $\boldsymbol{A}=\left[a_{ij}\right]_{n\times n}$, $\boldsymbol{f}(\boldsymbol{v})=\left[f_1(v_1)\cdots f_n(v_n)\right]^{\mathrm{T}}$, where $f_i(v_i)=K_i\left(\mathrm{e}^{\lambda v_i}-1\right)$ $i=1,\cdots,n$, are the currents flowing through all the diodes. Since K_i is a very small number, typically $K_i=10^{-14}$ A, function $f_i(v_i)$ is approximately equal to zero for v_i smaller than some positive threshold voltage w. If we choose $w=0.2$ then $\left|f_i(v_i)\right|<10^{-10}$ for $v_i<w$. Hence, it is justified to consider $f_i(v_i)$ as equal to zero for $v_i<w$, i.e. we assume

$$f_i(v_i)=\begin{cases} 0 & \text{for} \quad v_{\mathrm{i}}<w \\ K_i\left(\mathrm{e}^{\lambda v_i}-1\right) & \text{for} \quad v_i\geq w. \end{cases} \tag{5}$$

A method for finding all the solutions to Eq. (4) is sketched underneath.

We wish to find all the solutions to Eq. (4) which satisfy the constraints: $-E\leq v_i\leq E$, $0\leq i_i\leq I_i$, $i=1,\cdots,n$, where E is the sum of all voltage sources acting in the circuit, whereas I_i is the forward burnout current of i-th diode. Hence, taking into account Eq. (5) we obtain

$l_i^0\leq v_i\leq u_i^0$, where $l_i^0=-E$,

$u_i^0=\min\left\{E,\frac{1}{\lambda}\ln\left(\frac{I_i}{K_i}+1\right)\right\}$, $i=1,\cdots,n$. Thus, we seek all the solutions to Eq. (4) in the n-dimentional rectangular region $\left[\boldsymbol{l}^0,\boldsymbol{u}^0\right]=\left[l_1^0,u_1^0\right]\times\cdots\times\left[l_n^0,u_n^0\right]$, $l_i^0\leq v_i\leq u_i^0$, $i=1,\cdots,n$.

To find all the solutions we apply the idea of successive contraction, division, and elimination [4].

The crucial point of this approach is a contraction method described in detail in [4]. The main idea of this method is as follows.

Let us consider an arbitrary region $[\boldsymbol{l},\boldsymbol{u}]=[l_1,u_1]\times\cdots\times[l_n,u_n]$, $l_i \le v_i \le u_i$.

We frame each characteristic $f_i(v_i)$ for $v_i \in [l_i,u_i]$ $i=1,\cdots,n$, using two parallel straight lines, as it is illustrated in Fig. 1. Having determined all the slopes $s_1,\cdots,s_n$ and all the offsets $c_1^-,\cdots,c_n^-,c_1^+,\cdots,c_n^+$, we form the matrix

$$\boldsymbol{M}=\operatorname{diag}(s_1,\cdots,s_n) \tag{6}$$

and vectors $\boldsymbol{c}^-=\left[c_1^-\cdots c_n^-\right]^{\mathrm{T}}$, $\boldsymbol{c}^+=\left[c_1^+\cdots c_n^+\right]^{\mathrm{T}}$.

Let $\boldsymbol{v}^*$ be an arbitrary solution of equation (4) belonging to the region $[\boldsymbol{l},\boldsymbol{u}]$. Any component v_i^* of $\boldsymbol{v}^*$ be considered as a point which lies on the straight line $y_i=s_i v_i+c_i$, where

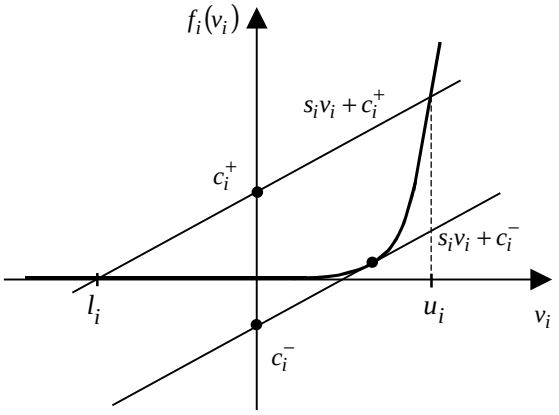

Fig. 1. Illustration of the contraction method

$c_i^- \le c_i \le c_i^+$. Hence, the linear equation

$$\boldsymbol{M}\boldsymbol{v}^*+\boldsymbol{c}+\boldsymbol{A}\boldsymbol{v}^*-\boldsymbol{b}=\boldsymbol{0} \tag{7}$$

arises, where components c_i $(i=1,\cdots,n)$ of vector $\boldsymbol{c}$ are unknown, but the bounds c_i^-, c_i^+ on them are given. Solving equation (7) for $\boldsymbol{v}^*$ we find

$$\boldsymbol{v}^*=\boldsymbol{Z}\boldsymbol{d}, \tag{8}$$

where $\boldsymbol{Z}=\left[z_{ij}\right]_{n\times n}=[\boldsymbol{M}+\boldsymbol{A}]^{-1}$, $\boldsymbol{d}=[d_1\ldots d_n]^T=\boldsymbol{b}-\boldsymbol{c}$

$d_i^-=b_i-c_i^+ \le d_i \le b_i-c_i^-=d_i^+$. Using (8) we find new bounds on $\boldsymbol{v}^*$, such that $p_i^- \le v_i^* \le p_i^+$, $i=1,\cdots,n$, where

$$p_i^-=\sum_{j=1}^{n} z_{ij}\alpha_j, \qquad p_i^+=\sum_{j=1}^{n} z_{ij}\beta_j, \quad \alpha_j=\begin{cases} d_j^+ & \text{if} \quad z_{ij}\le 0 \\ d_j^- & \text{if} \quad z_{ij}>0 \end{cases},$$

$$\beta_j=\begin{cases} d_j^+ & \text{if} \quad z_{ij}\ge 0 \\ d_j^- & \text{if} \quad z_{ij}<0 \end{cases}.$$

Next we define $l_i^1=\max\left\{l_i,p_i^-\right\}$, $u_i^1=\min\left\{u_i,p_i^+\right\}$ and form region $\left[\boldsymbol{l}^1,\boldsymbol{u}^1\right]\subset[\boldsymbol{l},\boldsymbol{u}]$, $\left(\boldsymbol{l}^1=\left[l_1^1\cdots l_n^1\right]^{\mathrm{T}}, \boldsymbol{u}^1=\left[u_1^1\cdots u_n^1\right]^{\mathrm{T}}\right)$ containing the same solutions as $[\boldsymbol{l},\boldsymbol{u}]$. The contraction is continued, leading to regions $\left[\boldsymbol{l}^2,\boldsymbol{u}^2\right]$, $\left[\boldsymbol{l}^3,\boldsymbol{u}^3\right]$, ...

If at any stage of the contraction process the lower bound overlaps the upper bound, for at least one component, i.e. $l_k^\mu > u_k^\mu$ for some μ and k, then we conclude that the region $[\boldsymbol{l},\boldsymbol{u}]$ contains no solution. In such a case this region is discarded.

To improve this method we take into account matrix equation (4), consisting of n scalar equations having the form

$$f_i(v_i)+\sum_{j=1}^{n} a_{ij}v_j=b_i, \quad i=1,\ldots,n. \tag{9}$$

Consider a region $[\boldsymbol{l},\boldsymbol{u}]=[l_1,u_1]\times\cdots\times[l_n,u_n]$, $(l_i \le v_i \le u_i, i=1,\cdots,n)$ and select a subset X^- of the set of equations (9) for which $u_i \le w$ (or $v_i \le w$). Without any loss of generality we assume that X^- consists of the first m equations of set (9). Consequently, the equations $f_1(v_1)=0,\cdots,f_m(v_m)=0$ hold. In such a case equation (4) can be rearranged to give

$$\begin{aligned} &\boldsymbol{A}_1\boldsymbol{v}_1+\boldsymbol{A}_2\boldsymbol{v}_2=\boldsymbol{b}_1, \\ &\boldsymbol{A}_3\boldsymbol{v}_1+\boldsymbol{A}_4\boldsymbol{v}_2+\boldsymbol{f}_2(\boldsymbol{v}_2)=\boldsymbol{b}_2, \end{aligned} \tag{10}$$

where $\boldsymbol{v}_1=\left[v_1\ldots v_m\right]^{\mathrm{T}}$, $\boldsymbol{v}_2=\left[v_{m+1}\ldots v_n\right]^{\mathrm{T}}$, $\boldsymbol{A}_1,\boldsymbol{A}_2,\boldsymbol{A}_3,\boldsymbol{A}_4$, are submatrices of $\boldsymbol{A}$, $\boldsymbol{b}_1=\left[b_1\ldots b_m\right]^{\mathrm{T}}$, $\boldsymbol{b}_2=\left[b_{m+1}\ldots b_n\right]^{\mathrm{T}}$, $\boldsymbol{f}_2(\boldsymbol{v}_2)=\left[f_{m+1}(\boldsymbol{v}_{m+1})\ldots f_n(\boldsymbol{v}_n)\right]^{\mathrm{T}}$.

By pivoting in succession on the diagonal elements of matrix $\boldsymbol{A}_1$ we rearrange equations (10) to

$$\boldsymbol{v}_1+\hat{\boldsymbol{A}}_2\boldsymbol{v}_2=\hat{\boldsymbol{b}}_1, \tag{11}$$

$$\boldsymbol{f}_2(\boldsymbol{v}_2)+\hat{\boldsymbol{A}}_4\boldsymbol{v}_2=\hat{\boldsymbol{b}}_2 \tag{12}$$

and apply the contraction method, described above.

The form of equations (11)-(12) enables us to frame only the scalar functions of the vector representation $\boldsymbol{f}_2(\boldsymbol{v}_2)$ and consequently reduce the size of matrices which are

inverted in the contraction process. Furthermore, inverting the matrices can be efficiently carried out using some matrix formulas. In this way the contraction method is considerably improved.

The contraction procedure, after appropriate modification, also can be applied to equation $\boldsymbol{i} = \boldsymbol{b} - \boldsymbol{A}\boldsymbol{v}$, where $\boldsymbol{i} = \boldsymbol{f}(\boldsymbol{v})$, considering n-dimensional rectangular regions relating to the current vector.

Some regions containing no solution can be straight-forwardly discarded using algorithms based on investigation of some selected scalar equations of the representation (4) and showing that any point of the considered region violates at least one of these equations. Two algorithms employing this idea, called direct algorithms, have been proposed.

The direct and contraction algorithms sketched above have been employed in the method for finding all the DC solutions, proposed in this paper. To find all the solutions in a given region we use the idea of successive contraction, division, and elimination. When the computation process is carried out many n-dimensional rectangular regions are considered. To each of them we first apply the direct algorithms. If the algorithms do not discard the region we use the improved contraction algorithms.

The algorithm developed in this paper is an important mathematical tool applied in the process of tracing the temperature characteristic. It enables us to find all values of the signal at any temperature belonging to the prescribed range. Each branch of the characteristic determines one of the values.

The proposed algorithm has been implemented in Delphi and tested on several electronic circuits using PC Pentium 4, 3 GHz.

Example 1

Figure 2 shows a circuit composed of two Schmitt's triggers [14]. The transistors are characterized by the Ebers-Moll model with resistors $R_B = 3\Omega$, $R_E = R_C = 10\Omega$. The parameters are as follows: $I_0 = 6.99732\,\text{fA}$, $\beta_{R_0} = 1\,\text{v}$, $\beta_{F_0} = 99$, $T_i = 3$, $T_\beta = 1.5$, $E_g = 1.11\,\text{eV}$. The temperature coefficients of the resistors are: $T_{C_1} = 2 \cdot 10^{-3}\,1/\text{K}$, $T_{C_2} = 0$. We wish to trace the temperature characteristic $v_{out} = F(T)$ for $T \in [10°\text{C}, 60°\text{C}]$.

Using the algorithm developed in this paper, with $\Delta T = 0.1°\text{C}$ we compute the characteristic shown in Fig. 3. It is composed of four disconnected branches, with two of them located very close one to another, hence, they cannot be distinguished in the figure.

The time consumed by the algorithm, is 1.2s. Using PSPICE simulator we obtain a fragmentary characteristic, containing only one branch, as shown in Fig. 4.

Example 2

Figure 5 shows a transistor circuit being a part of line receiver SN 75122. The transistors are characterized by the Ebers-Moll model with resistors $R_B = 3\Omega$, $R_E = R_C = 10\Omega$. The parameters are as follows:

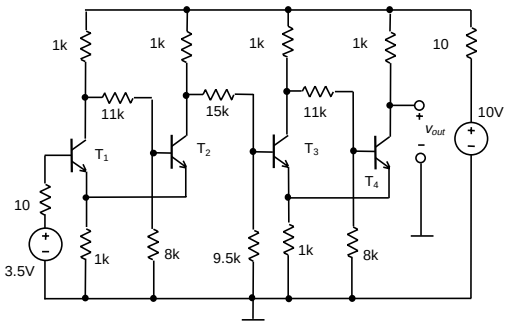

Fig. 2. Circuit composed of two Schmitt's triggers

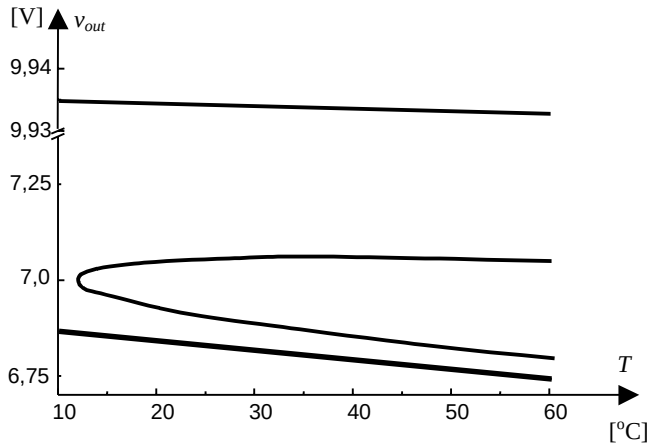

Fig. 3. Temperature characteristic $v_{out} = F(T)$ obtained using the proposed algorithm

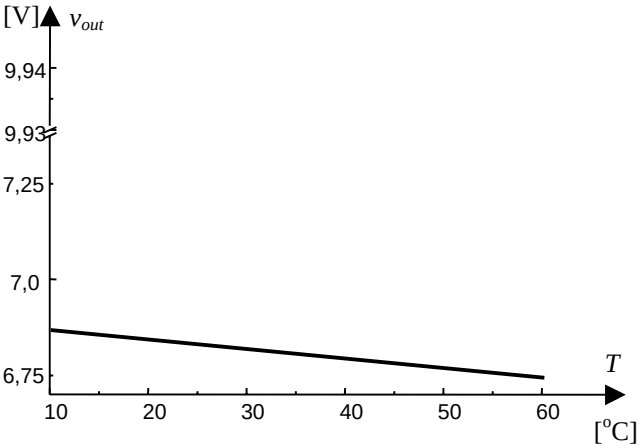

Fig. 4. Temperature characteristic $v_{out}=F(T)$ provided by SPICE

$I_0 = 7.049\,\text{fA}$, $\beta_{R_0} = 2.611$, $\beta_{F_0} = 375.5$, $T_i = 3$, $T_\beta = 1.5$, $E_g = 1.11\,\text{eV}$, $\eta = 1$. The temperature coefficients of the chip resistors are $T_{C_1} = 2 \cdot 10^{-3}\,1/\text{K}$, $T_{C_2} = 0$. We wish to find the temperature characteristic $v_{out} = F(T)$ for $T \in [20°\text{C}, 50°\text{C}]$ in two cases: $v_{in} = 1.5\,\text{V}$ and $v_{in} = 1.05\,\text{V}$. We use the algorithm developed in this paper, with $\Delta T = 0.1°\text{C}$.

Figure 6 shows the obtained characteristic for $v_{in} = 1.5\,\text{V}$. The time consumed by the algorithm is 11.5s. The characteristic provided by SPICE is incomplete, it contains only one branch, as it is shown in Fig. 7. The characteristic obtained by the proposed algorithm and SPICE, at $v_{in} = 1.05\,\text{V}$, are shown in Figs. 8 and 9, respectively. A comparison of the characteristics manifests that SPICE gives a fragmentary characteristic. The time consumed by the proposed algorithm is 15.3s.

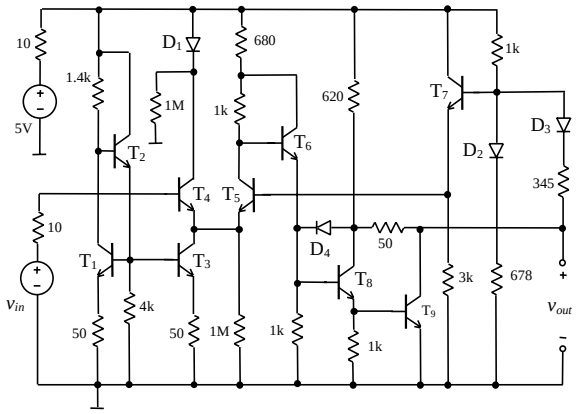

Fig. 5. Diode-transistor circuit for Example 2

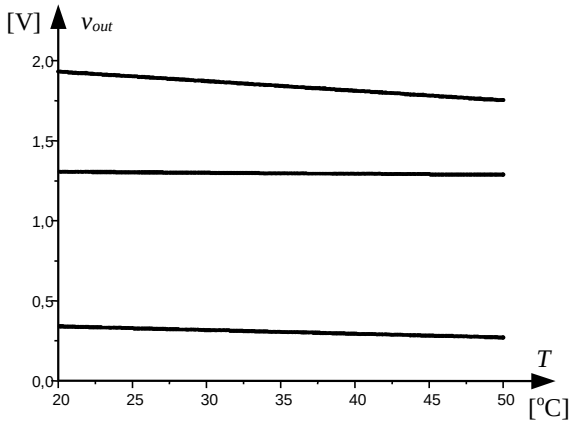

Fig. 6. Temperature characteristic of the circuit shown in Fig. 5, at $v_{in} = 1.5\,\text{V}$, obtained using the proposed algorithm

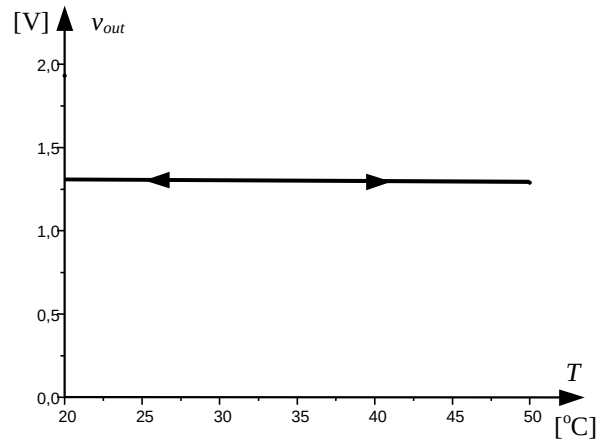

Fig. 7. Temperature characteristic of the circuit shown in Fig. 5, at $v_{in} = 1.5\,\text{V}$, provided by SPICE

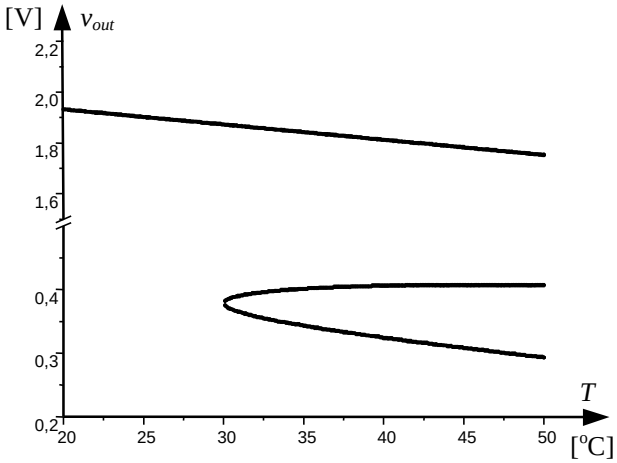

Fig. 8. Temperature characteristic of the circuit shown in Fig. 5, at $v_{in} = 1.05\,\text{V}$, obtained using the proposed algorithm

3. Temperature characteristics of circuits containing thermistors

Consider a transistor circuit, as defined in Section 2, including additionally a thermistor. The thermistor is considered as a resistor, connected to the chip, depending on temperature, described by equation $\hat{v} = R_h(T)\hat{i}$. Assume that the temperature of the chip is constant, whereas the temperature of the thermistor varies in interval $\left[T^-, T^+\right]$.

To describe the circuit we modify the Sandberg-Willson equation by introducing a term depending on the thermistor voltage

$$\boldsymbol{\Gamma f}(\boldsymbol{v}) + \boldsymbol{G}_{11}\boldsymbol{v} + \boldsymbol{G}_{12}\hat{v} - \boldsymbol{d} = \boldsymbol{0}, \tag{13}$$

where $\boldsymbol{G}_{11}$ is (nxn) matrix as in Eqs. (1), $\boldsymbol{G}_{12}$ is an $(nx1)$ matrix. Furthermore, we formulate additional equation expressing the thermistor current in terms of $\hat{v}$, $\boldsymbol{v}$, and independent sources acting in the circuit

$$\hat{i} = \hat{d} - \boldsymbol{G}_{21}\boldsymbol{v} - G_{22}\hat{v}, \tag{14}$$

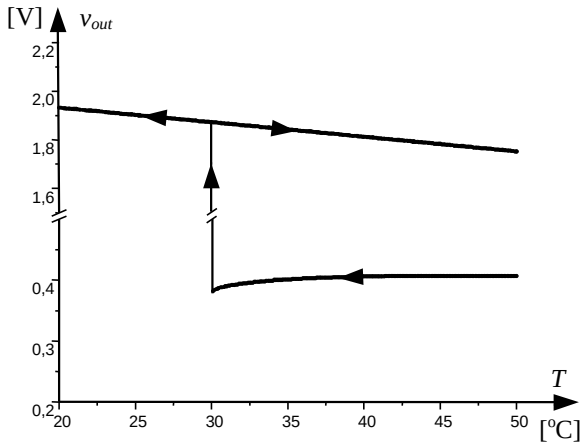

Fig. 9. Temperature characteristic of the circuit shown in Fig. 5, at $v_{in} = 1.05\,\mathrm{V}$, provided by SPICE

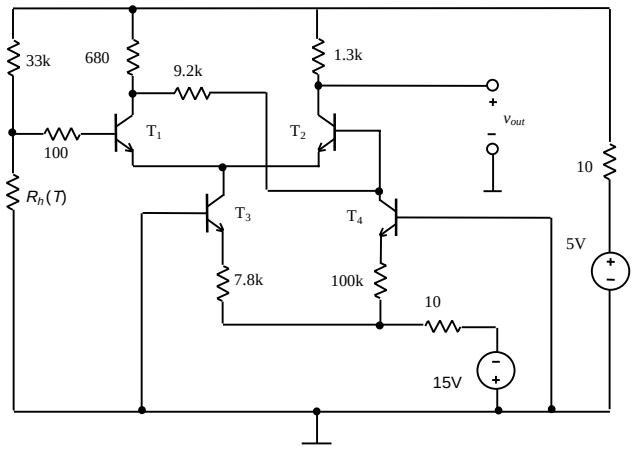

Fig. 10. A circuit containing thermistor $R_h(T)$

where $\boldsymbol{G}_{21}$ is a $(1xn)$ matrix. On the other hand

$$\hat{i} = R_h^{-1}(T)\hat{v}. \tag{15}$$

Rearranging equations (13)-(15), yields

$$\boldsymbol{f}(\boldsymbol{v}) + \hat{\boldsymbol{A}}(T)\boldsymbol{v} - \boldsymbol{c}(T) = \boldsymbol{0}, \tag{16}$$

where

$$\hat{\boldsymbol{A}}(T) = \boldsymbol{\Gamma}^{-1}\left(\boldsymbol{G}_{11} - \boldsymbol{G}_{12}\left(R_h^{-1}(T) + G_{22}\right)^{-1}\boldsymbol{G}_{21}\right),$$

$$\boldsymbol{c}(T) = \boldsymbol{\Gamma}^{-1}\left(\boldsymbol{d} - \boldsymbol{G}_{12}\left(R_h^{-1}(T) + G_{22}\right)^{-1}\hat{d}\right).$$

The algorithm developed in Section 2 applied to equation (16) enables us to find characteristic $y = \hat{F}(T)$, where T is the temperature of the thermistor.

Example 3

Let us consider the circuit shown in Fig. 10, including NTC thermistor $R_h(T)$ [14]. The transistors are characterized by the Ebers-Moll model with resistors: $R_B = 3\Omega$, $R_E = R_C = 1\Omega$, and parameters: $I_0 = 7.049\,\mathrm{fA}$, $\beta_{R_0} = 1$, $\beta_{F_0} = 99$.

The chip is at fixed temperature T=27°C, hence, its parameters are constant. We wish to trace the characteristic $v_{out} = \hat{F}(T)$, where the thermistor temperature T belongs to the interval [10°C, 100°C]. Using the algorithm developed in Section 3, we obtain the characteristic shown in Fig. 11. The time consumed by the algorithm is 1.6s. The characteristic given by SPICE (ICAP 4 or PSPICE) is presented in Fig. 12. The latter exhibits apparent hysteresis. The method developed in this paper guarantees finding all the DC solutions at any temperature. Figure 11 shows that for $T \in [T', T'']$ there are three solutions. The characteristic depicted in Fig. 12 gives, in this range, only two of them.

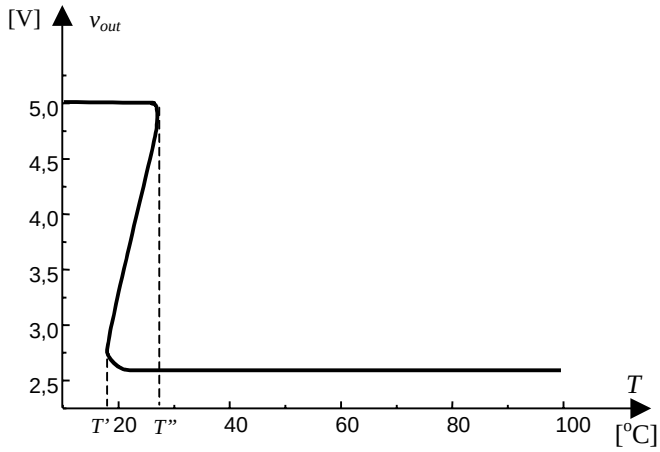

Fig. 11. The characteristic $v_{out} = \hat{F}(T)$ obtained using the proposed algorithm

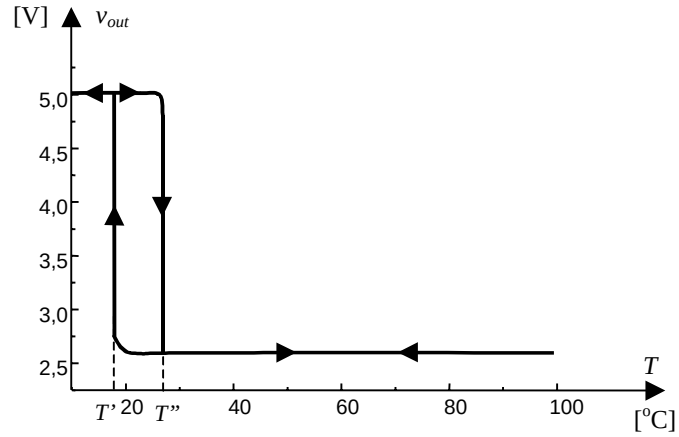

Fig. 12. The characteristic $v_{out} = \hat{F}(T)$ provided by SPICE

4. Conclusions

The algorithm for tracing the temperature characteristics of diode-transistor circuits having multiple DC solutions is efficient. It gives complete characteristics, which are multivalued and usually composed of disconnected branches. The characteristics are necessary in the analysis of the circuits, considering thermal behavior of the chip [15]. On the other hand, the characteristics provided by SPICE are fragmentary, lose some branches or exhibit apparent hysteresis.

The proposed approach also can be directly applied to circuits containing MOS transistors, characterized by the Shichman-Hodges model. Application to short-channel MOSFET circuits requires modification of the method for finding all the DC solutions in circuits with constant parameters.

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